Relative Ultrasound Energy Measurement Circuit

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Abstract – A relative ultrasound energy estimation circuit has been designed in a standard 0.35- μm CMOS process, to be a part of a thumb size internet connected wireless ultrasound measurement system. This circuit measures the relative energy between received ultrasound pulses, and presents an output signal that is linear to the received energy. Post-layout simulations indicate 7 bit linearity for 500 mV input signals, 5 μsec startup and stop times, 2.6 mW power consumption during active state. The active area measures 0.6 mm² including digital logic, bias generation, and an on-chip oscillator. The circuit has been sent for manufacturing in the austrianmicrosystems C35B4 process via Europractice MPW.

Keywords – Ultrasound, Piezo-electric crystal, CMOS, Measurement.

I. INTRODUCTION

Ultrasound is used today in many different fields, such as health care, medicine, and within the industry. Measurement applications using ultrasound are flow meters, liquid level detection, or fatigue crack detection in aircraft materials. Ultrasound expands into many new industry driven areas and cost of production and cost of installation are issues for many ultrasound systems of today. There is a drive to make these systems small, mobile, wireless, internet connected and battery operated. One step on the way to decrease the system size and power consumption is to develop electronics, custom made to be integrated close to the ultrasound crystal [1] [2] [3] [4] [5]. A thumb size wireless platform could be used for data processing, communication, and online presentation of measurement data [6] [7].

If material properties are to be determined with ultrasound, there are two available approaches, either time of flight measurements or energy/amplitude measurements. The energy measurements have traditionally been done with a high speed analog to digital converter and a microprocessor to gather data and compute the results.

This paper investigates if analog signal processing can be used to estimate the relative energy of ultrasound echoes, for less power compared to its traditional counterpart. One possible system block diagram can be seen in Figure 1. Here the blocks circumferenced by the dashed line is presented in [5] and the microprocessor system circumferenced by the dash-dotted line

is presented in [6]. The energy estimation can also be divided into two blocks, as illustrated in Figure 2. There are previous reports of peak detectors [9] and precision rectifiers [10]. These are used as a foundation for the rectifier design.

Fig. 1. THE COMPLETE RECEIVING SYSTEM. THE ENERGY ESTIMATION BLOCK IS PRESENTED IN THIS PAPER

Fig. 2. THE BLOCK DIAGRAM OF THE ENERGY ESTIMATION SYSTEM WITH NOISE SOURCES

II. SPECIFICATION AND THEORY

A. System specification

For a typical ultrasound measurement system using the energy/amplitude as primary parameter, the specifications presented in Table I are appropriate.

A basic system architecture for the analog signal processing approach is presented in Figure 1.

The system architecture and the specifications in Table I give rise to the following design considerations.

The input signal amplitude from a typical ultrasound measurement system has a variation that depends on the measurement situation. This variation can be as large as a factor of four [11]. A realistic system input signal could be

set to maximal 75 percent of the supply voltage. The power supply V_{DD} is set according to the specification of a standard CMOS process. The system bandwidth is dimensioned to suite a piezoceramic disc with a center frequency of 4 MHz. The startup-time is a compromise between power consumption and speed. A slow startup time was set as a design target. A power consumption estimate of a traditional high speed analog to digital converter (ADC) could be used to set the specification of this system. A 10-bit, 10 MSample ADC can be estimated to consume about 20 mW [8], and a reasonable design goal is to decrease this by a factor of two.

The equivalent input noise specification that can be seen in Table I is defined for a 2.5 V signal swing, and 10 bits of analog to digital conversion. The quantization RMS noise of an analog to digital converter is found as $V_{n,Q} = \frac{LSB_{ADC}}{\sqrt{12}}$.

TABLE I.
CIRCUIT SPECIFICATION

Design object	Design goal
Accuracy	10 bit
$v_{in,max}$	2.5 V peak to peak
V_{DD}	3.3 V
Input bandwidth	10 MHz
Startup time	< 5 μ sec
Integrated power consumption	< 10 mW
Output noise voltage RMS	< 705 μ V RMS
Output load	10 pF

B. Noise theory

The energy W of a time domain voltage signal $v_{in}(t)$ can be found if the power of this signal developed in a conductance G is integrated over time T .

$$W = G \int_0^T v_{in}(t)^2 dt \quad (1)$$

When an electronic system is to be designed two different noise voltage $v_{n1}(t)$ and $v_{n2}(t)$ could be introduced. The first noise voltage represents the inherited signal noise which is received by the system. The second noise voltage represents the uncorrelated noise created within the system itself, but recalculated to equivalent input noise. This is also illustrated in Figure 2. The energy expression can be found as

$$W_{tot} = G \int_0^T ((v_{in}(t) + v_{n1}(t))^2 + v_{n2}(t)^2) dt. \quad (2)$$

Assuming that the noise energy W_{n2} is constant over time it follows that

$$W_{n2} = G \int_{T_0}^{T_1} (v_{n2}(t)^2) dt = G \int_{T_2}^{T_3} (v_{n2}(t)^2) dt, \quad (3)$$

if $(T_1 - T_0) = (T_3 - T_2)$ and if $(T_1 - T_0)$ is large. Thus if the noise energy could be measured for the same duration, at

a later instance in time, the results could be approximated as equal. This is only valid if the integration times are long in comparison to the longest regarded noise period time. If a later noise integration could be subtracted from the energy expressed in Equation 2, only the correlated noise energy would remain. This can be expressed as

$$W_{n,remainder} = 2G \int_{T_0}^{T_1} (v_{in}(t)v_{n1}(t)) dt + G \int_{T_0}^{T_1} (v_{n1}(t)^2) dt. \quad (4)$$

There are cases where the noise voltage $v_{n1}(t)$ also can be regarded as uncorrelated from the signal. In those cases, the noise voltage $v_{n1}(t)$ can be neglected in the analysis.

C. Signal theory

The input signal to this system designated $v_{in}(t)$ in Figure 3, is amplified in one inverting unity-gain amplifier to produce the system signal $v_{neg}(t)$, and one non-inverting unity-gain amplifier to create the signal $v_{pos}(t)$.

Fig. 3. A DETAILED BLOCK DIAGRAM OF ENERGY ESTIMATION SYSTEM

Each of the signals $v_{pos}(t)$ and $v_{neg}(t)$ are connected with a coupling capacitor into a capacitive input of a half wave rectifier. There will be a voltage division of the two signals $v_{pos}(t)$ and $v_{neg}(t)$ depending on the size of these capacitors, and the effective input energy is reduced by a factor of

$$k_{input} = \left(\frac{C_{c,rect}}{C_{in,rect} + C_{c,rect}} \right)^2. \quad (5)$$

Here the $C_{c,rect}$ is the size of the coupling capacitor and $C_{in,rect}$ is the size of the input capacitance of a half-wave rectifier.

The rectifier input voltages $v_{POS}(t)$ and $v_{NEG}(t)$ in Figure 5 are biased with an overdrive V_{OD} , to assure that the input devices will be operating with strong inversion in the channel. The input transistor drain voltage is also dimensioned to keep the rectifier input transistors in the saturation region for small input voltages. This implies that the large signal current of the rectifier input transistors will follow the large signal drain current relation

$$i_{D,pos}(t) = \frac{\mu C_{ox} W}{2L} (v_{pos}(t) + V_{OD})^2, \quad (6)$$

for the positive side. The relation

$$i_{D,neg}(t) = \frac{\mu C_{ox} W}{2L} (-v_{pos}(t) + V_{OD})^2, \quad (7)$$

can be applied for the negative side. When the two currents are added the signal current becomes

$$i_{signal}(t) = \frac{\mu C_{ox} W}{L} (v_{pos}(t))^2. \quad (8)$$

Along with this current, a bias current of

$$I_{D,bias} = \frac{\mu C_{ox} W}{L} (V_{OD})^2, \quad (9)$$

is also created. The current i_{signal} is fed to a capacitor C_{out} on the output to perform the integration. The relation

$$V_{out}(t) = \int_0^T \frac{i(t)}{C_{out}} dt \quad (10)$$

connects time and current to voltage and capacitance. Thus the system transfer function voltage $V_{out}(t)$ after a time T can be found as

$$V_{out} = \frac{k_{rect} k_{input} \mu C_{ox} W}{L C_{out}} \int_0^T (v_{pos}(t))^2 dt, \quad (11)$$

where a rectifier efficiency k_{rect} is defined. To estimate the system transfer function an input signal of

$$v_{in}(t) = A e^{-\alpha t} \sin(2\pi f t), \quad (12)$$

can be assumed, where the attenuation α , the amplitude A and the frequency f are specified. With the use of Equation 11 and Equation 12, an ideal output voltage can be found for different input amplitudes.

D. Design environment

The design environment that was used for this design is the Cadence environment and HIT-KIT, provided by austrianmicrosystems (AMS). The target process is a 0.35 μm standard CMOS process. For the on-chip glue logic, the Synopsis tools were used. Layout was done in Virtuoso provided by the Cadence environment.

III. CIRCUIT DESIGN

A. Implemented system details

A detailed block diagram can be seen in Figure 3. A typical operating condition can be seen in Figure 4. The inverting and non-inverting amplifiers create the differential input voltages $v_{pos}(t)$ and $v_{neg}(t)$ needed to get the full-wave rectification out of the two half-wave rectifiers. Section B above indicate that the effect of the integrated noise energy can be reduced if the system noise is integrated two times, and the results subtracted. This was incorporated in the system design.

Fig. 4. AN EXAMPLE OPERATION CONDITION, WITH A 4 MHz EXPONENTIALLY ATTENUATED SINUSOIDAL INPUT

B. Details of implemented amplifier

A standard Miller compensated Operational Transconductance Amplifier (OTA) was implemented with the simulation results seen in Table II. The performance listed in Table II are all worst case conditions simulated over the recommended process corners from AMS. The OTA is used to design two unity gain voltage amplifiers, one non-inverting and one inverting amplifier. Both of these amplifiers are implemented with capacitive feedback elements.

TABLE II.
OTA SIMULATION RESULTS

Specified entity	Simulated results
Unity Gain Bandwidth	10 MHz
Phase margin	60°
Output signal range	0.8 - 2.5 V
Equivalent input noise	1.3 nV per rootHz
Current consumption	550 μA
Startup time	2 μs
Occupied area	0.044 mm ²

C. Details of implemented rectifier

The rectifier principle schematic is illustrated in Figure 5. The current sources designated I_B supplies the bias current for the input devices $MN0$ and $MN1$. As the signal part $v_{pos}(t)$ of the input voltage $v_{POS}(t)$ increases, the signal current begin to increase through $MN1$, according to the large signal saturation current of an NMOS transistor. This signal current will be pulled out of the branch with $MP2$ and $MP4$, creating the rectified half wave signal.

D. Integrator

The signal current created in $MP4$ in Figure 5 is mirrored to $MP5$. Besides the overdrive bias current defined in Equation 9, the $MP5$ also requires a bias current. To keep either of these two bias currents from charging the capacitor on the output, an equal

Fig. 5. RECTIFIER PRINCIPLE SCHEMATIC

current is created using an identical structure as in Figure 5. This current is pulled out of the output, and it is designated the ideal current source I_{DC} in Figure 5. Even if the matching between these currents are not optimal, a DC offset could be removed along with parts of the uncorrelated noise, as suggested in Section B, by a reference integration without the input signal $v_{in}(t)$.

The bias current of an NMOS transistor depends on both V_{GS} and V_{DS} . Here V_{DS} will be determined by the output voltage $v_{OUT}(t)$. The drain current of an NMOS device increases with increasing V_{DS} . As for the PMOS transistor $MP5$, the drain current decreases when the $v_{OUT}(t)$ increases. This implies that the mismatch in drain currents of the current source and the $MP5$ will depend on the output voltage $v_{OUT}(t)$. This mismatch will be strong if the output voltage approaches the vicinity of the supply rails. This mismatch will cause nonlinearities in the system transfer function.

To minimize the required number of external components, an internal inter-poly capacitor structure of 10 pF in typical mean conditions was used as output capacitor. It is sized to integrate many echoes, to allow mean value correction. The integrator can be seen in Figure 5, as transistor $MP5$ and the ideal current source, with the current I_{DC} .

E. Charge injection

Charge injection is an issue that is familiar to most electronic designers. It is also a topic into which a significant effort has been spent. There are several reports of different compensation techniques [12], [13]. In this work, the Common Mode Rejection Ratio (CMRR) is high in all the included structures. Electrically equal paths have been used for all the signals that is passed over the circuit, and this reduces the issue with charge injection to a question of matching of components and signal paths, and to preserve a high CMRR throughout the circuit.

F. Details of additional electronics

The additional electronics required to make this chip self-contained are a voltage reference, an oscillator, some digital logic and an auto-zero compensation scheme for the amplifiers. The voltage reference is a standard resistor based reference [14]. The on-chip oscillator is implemented as a seven delay-element ring oscillator. The inverting and non-inverting amplifiers have an auto-zero phase, initially suggested by [15], implemented with an OTA as described in [16].

G. Layout

The layout is presented in Figure 8 with a floorplan. The size of the total ASIC is 1.7 mm by 1.3 mm.

H. Simulation results

Post-layout simulations were made to evaluate the design. A rectification of an exponentially attenuated sinusoidal input of 800 mV peak amplitude can be seen in Figure 4. One can see that there is distortion in the rectified current. This distortion will decrease the linearity as well as the efficiency of the rectification.

To estimate the efficiency and the accuracy of the structure, the amplitude was swept between 0 V and up to 500 mV, for ten equal exponentially attenuated sinusoids, and the result was sampled at the output. The input energy was determined using Equation 1, and the result can be seen in Figure 6.

Fig. 6. OUTPUT VOLTAGE CHANGE FROM A DC LEVEL PLOTTED VERSUS INPUT ENERGY OF 4 MHz EXPONENTIALLY ATTENUATED SINUSOIDS

A best-fit straight line starting at origo was fitted to the curve in Figure 6, and the difference between the output voltage and this line was divided with the maximum output signal. The results can be seen in Figure 7, which indicate 7.2 bit linearity

over the input signals up to 525 mV, thus 3.5 mV accuracy. The 500 mV only corresponds only to a fifth of the specified input signal range. It would require an ADC of 9.5 bits over 2.5 V to resolve 3.5 mV.

The main limitation on the input signal swing are the input devices $MN0$ and $MN1$ in Figure 5. A larger signal swing would require a different overdrive voltage, as well as a larger bias current through I_B . A larger input signal will today cause the input transistors $MN0$ and $MN1$ to go out of strong inversion, causing distortion in the output current waveform. A second source of non-linearity is the output voltage dependence of the bias current of the output transistor $MP5$.

Fig. 7. ERROR IN MV FOR BEST-FIT LINEARIZATION FOR POST LAYOUT SIMULATIONS

Theoretical integration of the input signal conditions with ten waveforms, with the use of Equation 11 and Equation 12 displayed an output voltage difference of 1.432 V at 4 MHz frequency, 500 mV amplitude, and an attenuation of $\alpha = 10^6$ where only about 270 mV came out which result in a $k_{rect} = 0.20$. This depends on the low impedance node between the transistors $MP1$ and $MN2$. This should ideally have had a high impedance.

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V. DISCUSSION

This paper has presented the post-layout simulation results from a new relative ultrasound energy measurement device. This device is to be integrated in the work towards the internet connected thumb-size ultrasonic measurement system. This

preliminary data indicate that energy measurements can be made, without the need of high speed conversions. The simulations were done on post-layout netlists, and they indicate that 7 bit linearity can be reached over an input swing of 500 mV. This is one bit less compared to a traditional high speed ADC system, but to less than a tenth of the power consumption.

The linearity is something that this topology struggles with, and a different rectifier principle could help things to improve. The price one has to pay for this is probably power consumption, which still is far away from the traditional system. The circuit has been sent for manufacturing in a standard 0.35 μm CMOS process. The next step is to validate the performance with measurements.

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Fig. 8. LAYOUT AND FLOORPLAN OF ASIC