EM Simulation of Planar Bus Bars in Multi-Level Power Converters

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Abstract

This paper presents recent progress in the acceleration of PEEC based electromagnetic simulations and its impact on the design of complex bus bar structures as used in multi-level power converters. The approach presented consists of different dedicated acceleration methods for the different design tasks. The first acceleration technique applied is the so called reluctance matrix method for full 3D field results, reducing memory consumption by orders of magnitude and computing time by a factor 3 to 5. The second acceleration method applied is based on model order reduction techniques for port-to-port impedance extraction, reducing the computation time by about one order of magnitude and allowing wideband macro modeling for system level simulations. The paper focuses on the application of these methods showing the impact on practical bus bar design tasks.

1. Introduction

Today, most frequency converters and motor drives in the medium voltage range are using multilevel topologies such as NPC (neutral point clamped) [1] and ANPC (active neutral point clamped) [2] (Figure 1). The reason for using multilevel topologies is to reduce the total harmonic distortions (THD) on the power lines and therefore lowering the need for filtering. In addition, these topologies also allow reaching higher voltages with low voltage devices, which in turn have the advantage of faster turn-on and turn-off switching times and therefore reduced switching losses. Disadvantages are the increased dI/dt and dV/dt , leading to new challenges in the electromagnetic design of products: A high dI/dt in combination with high stray inductances in the commutation paths leads to overvoltages that can destroy sensitive components (i.e. IGBTs). A high dV/dt requires better control of common mode noise propagation and general EMC noise emission. Finally, resonances between stray capacitances of the devices and stray inductances of the bus bar can lead to oscillations and ringing. In the near future, new fast switching wide bandgap devices (i.e. SiC and GaN) will further emphasize these issues [3][4]. Therefore, advanced EM simulation methods become a necessary tool in the design phase of multi-level power converter.

In literature, several bus bar simulation methods have been presented and their effectiveness proven [5]-[8]. Major drawback of most methods is that the computation effort and memory demand is getting prohibitively large for complex bus bars or when accurate and fast bus bar macro models are needed for system level simulations. In [8], bus bar simulations using the PEEC [9] method were presented where the so called divide-and-conquer approach was proven to be able to solve the large problems. This was possible because the bus bar had a regular structure of repeating identical elements, arranged in a row with negligible coupling. In this work we are investigating a different type of bus bars, with less regular structures and more complex layouts, hence simplification methods such as 'divide-and-conquer' can no longer be applied (Figure 2). The paper is therefore evaluating the potential of a simulation methodology based on two numerically accelerated PEEC solving variants, dedicated to different typical bus bar design tasks.

Figure 1: Examples of multi-level topologies, demanding complex bus bars: NPC (a) and ANPC (b).

Figure 2: Photograph of actual bus bar of one phase building block of a medium voltage multi-level converter.

Section 2 introduces the case study bus bar with the different design tasks. Section 3 describes the simulation methodology and shortly explains the acceleration methods applied. The Sections 4 and 5 explain the bus bar modeling and compare it to reference measurements. Section 6 presents the results and discusses the potential of the methodology. Section 7 finally draws the conclusions.

2. Problem Description

The bus bar investigated in this work is interconnecting in one phase building block a total of 12 IGBT power modules with two switches each. Three phase building blocks are forming one three-phase inverter. Pairs of IGBT modules are parallel connected in order to double the total current rating of the converter.

The positioning of the IGBT modules is mainly driven by the cooling design, requiring equal distribution of the power losses on the heat sink they are attached to. Consequence of this design are spatially spread modules with long interconnect distances. Goal of the bus bar design is therefore to minimize the stray inductance L_σ of all the critical commutation loops. The critical commutation loops can be identified based on the topology's switching scheme, which is however not subject of this paper.

A second critical design task relevant in this particular case is the symmetric on-state and dynamic current distribution between the paralleled IGBT power modules. Any asymmetry would lead to unequal thermal stress and consequently to accelerated component ageing.

Finally, the bus bar should be as small and light weight as possible to keep costs low, but without creating thermal hot spots caused by high current densities. The layout must therefore be designed such as to avoid current crowding in corners and edges and provide enough cross section where high currents are flowing.

3. Simulation Methodology

Different modeling and simulation approaches are needed to take into account the electrical design considerations presented in the previous section. Figure 3 shows the simulation flow adopted in this work. Common to all simulation tasks is to start with a Partial Element Equivalent Circuits model of the bus bar geometry (Figure 4) and to create a matrix formulation of the model. For the following steps, two options exist, depending on whether 3D field results are needed or not.

3D field solution with reluctance matrix PEEC solver

The first option is used when the simulation results are expected to provide 3D field information. Typically these are current density distributions and magnetic field patterns. In this case, also impedance curves can be gained from the simulation results. However, since (R, L_p) PEEC matrices

can become very large, a dedicated acceleration techniques based on the reluctance matrix method [10] has been developed and applied to the PEEC solver.

In this approach, the partial reluctance matrix is calculated by inverting the partial inductance matrix. The problem of inverting large partial inductance matrices, which arise from complex problems in PEEC, has been overcome by grouping the structure on each geometrical axis. As a result, the partial inductance matrix will be in block diagonal form where each block can efficiently be inverted to calculate the partial reluctance values.

The achieved partial reluctance matrix is strictly diagonally dominant and can therefore be safely sparsified by eliminating small couplings and still keep the solution acceptably accurate [11]. Further, by having sparser systems, the needed memory will be reduced and it will be possible to utilize sparse direct solvers [12], which can solve the equation more efficiently and in less time.

Figure 3: Modeling and simulation flow for different tasks.

Figure 4: 3D PEEC model of phase module bus bar.

Behavioral solution with MOR technique

The second option applies to the case where the 3D field results are not required. This is for example true when only impedances and coupling coefficients are analyzed or when macro models for system level simulations are created. In this case, model order reduction (MOR) techniques can be applied to the matrix to compute behavioral port solutions. This method is faster by orders of magnitude compared to the full matrix solving of large problems [15].

Assuming that the full (R,L,P)PEEC model admits a N -dimensional realization in the descriptor state-space form

$$E\dot{x} = Ax + Bu \quad (1a)$$

$$y = Cx \quad (1b)$$

a basic approach to constructing passive reduced-order models is to employ a projection matrix V_n of rank n such that

$$A_n = V_n^T A V_n \quad E_n = V_n^T E V_n \quad B_n = V_n^T B \quad C_n = C V_n$$

Hence, the reduced order model is obtained as a projection of the N -dimensional state space of the original system into the n -dimensional subspace spanned by the columns of the matrix V_n , provided that $n \ll N$. The projection approach can be efficiently combined with the use of Krylov subspaces to obtain reduced-order models that are passive and, at the same time, satisfy a moment-matching property [15]. To this end, the projection matrix is chosen as a basis of the Krylov subspace of order n . The corresponding reduced order model is the one produced by the PRIMA algorithm [15].

4. Case Study Modeling

Figure 4 in the previous section introduced the geometry of the bus bar model. The model and the model discretization (meshing) have been prepared for the faster orthogonal implementation of the MultiPEEC solver [13]. For this, almost no simplification or staircasing was needed due to the mainly orthogonal design of the actual bus bar (see photograph in Figure 2). Two important modeling aspects are discussed in the following sub-section: How to include the IGBT modules, which are part of the commutation paths, and how to discretize the thin copper sheets of the bus bar to account for skin and proximity effects.

IGBT module equivalents

The actual IGBT modules consist of several power semiconductor chips (IGBTs and antiparallel diodes) attached and wire bonded to a ceramic substrate with copper traces and power terminals. In order to clearly separate the contributions of the bus bar and the modules to the total loop impedance, we decided to replace the modules with short circuits at the terminal locations. The short circuits were therefore modeled with short bar element as shown in Figure 5. The cross-section and the

equivalent ohmic resistance ($200 \mu\Omega$) of the bars were chosen such as to match the real short circuit parameters used in the verification measurements (see Section 5).

Figure 5: 3D model with IGBT modules (a) and with IGBT module replaced by a short circuiting/resistive bar (b).

Cooper sheet modeling

The actual copper thickness is 1 mm, which corresponds to about twice the skin depth in a copper wire at 20 kHz, which is in the range of our frequencies of interest. Therefore it becomes very crucial to choose an appropriate thickness discretization to correctly take into account skin and proximity effects. Four different meshing variants were therefore investigated (Figure 6).

Figure 6: Thickness meshing variants for busbar copper layers.

Table 1: List of bus bar model variants simulated.

Model label	Thickness [mm]	Mesh [layers]	Non-uniformity [ratio]	Unknowns [-]
M-1-10	1	1	n/a	7'924
M-1-32	1	3	1:2	33'276
M-1-34	1	3	1:4	33'276
M-1-52	1	5	1:2	58'644

In variant a) the discretization is set to zero, which means that the current is flowing in a 2D plane. This variant covers the DC and low frequency cases, where uniform cross sectional current density can be assumed. In the variants b) to d), non-uniform thickness discretization is chosen, which means that the mesh is getting denser towards the surface, in a similar way as the current density increases with higher frequency. This way, the skin effect is

taken into account up to the frequency where the skin depth matches the outermost mesh thickness. The variants b) and c) subdivide the thickness in 3 layers with two different non-uniformity values. Variant d) divides the thickness in 5 layers. Table 1 lists the five resulting model variants with the corresponding labels and parameters.

5. Reference Measurements

For verification purposes, reference measurements of the actual bus bar impedances were performed. An Agilent 4294A impedance analyzer with open/short calibration was used (Figure 7a).

Figure 7: Measurement setup with bus bar and impedance analyzer (a) and short circuit bars (b).

The elements that were used in the simulation model to short circuit the IGBT module terminals were implemented as copper bars screwed to the bus bar connectors (Figure 7b). The cross-section of the bars and the residual resistance of the non-ideal short circuit (bars and screw interfaces) were measured and used in the simulation models (see Section 4). The frequency plots in Figure 8 show the inductance and resistance values extracted from the impedance measurement. As can be seen from the curves, at low frequencies the sensitivity of the measurement setup is getting too low to accurately extract the equivalent inductance. For that reason, the comparisons will be done for the frequency range of 1 kHz to 1 MHz.

Figure 8: Inductance and resistance measurement plots, illustrating the sensitivity limitations at lower frequencies.

6. Simulations Results

Impedance analysis with reluctance matrix PEEC solver

First, we analyze the results of the impedance simulation and the extraction of resistance and inductance. Figure 9 and Figure 10 show the results obtained with the full (R, L_p, P) PEEC solver, compared to the reference measurements. For the inductances (Figure 9), an accuracy of better than 10% is achieved throughout the frequency range of interest, without significant differences between the four discretization levels. In the case of resistances (Figure 10) the results are more differentiated but still as expected: The case without thickness discretization (M-1-00S) shows a rather flat frequency dependency, which is well matching the DC/LF measurements, but which is not able to represent the characteristic resistance increase.

Increasing the outer mesh density (cases M-1-32, M-1-34 and M-1-52) significantly improves simulation accuracy at high frequency. What can be observed is that increasing the non-uniformity ratio (M-1-34) brings more improvement than increasing the discretization (M-1-52).

Figure 9: Comparison of measured and simulated inductance.

Figure 10: Comparison of measured and simulated resistance.

Impedance analysis with MOR PEEC

Figure 11 shows the inductance and resistance curves obtained with the model order reduction technique, compared to the non-reduced simulations. As can be seen, the reduction method applied provides the same results as the full (R, L_p, P) PEEC, hence with the same frequency behavior and the same accuracy.

Figure 11: Inductance and resistance values obtained using standard PEEC and PEEC with model order reduction.

Direct time and memory comparisons are not fully fair at this point, since the (R, L_p, P) PEEC simulations were run with a compiled C++ code, using a multi-core supported math library while the MOR simulations were performed on Matlab. Nonetheless, the comparison numbers in Table 2 still show that the MOR technique has its clear benefits for this type of simulations, especially regarding the solution time. In this example, however, the impedance between only two terminals (nodes) was computed. In the case of multiple ports, the model order reduction effort increases with the number of terminals, while in the case of the full (R, L_p, P) PEEC the effort stays the same. Future studies will therefore be investigating the scaling rules for multi-terminal MOR.

Table 2: Computation performance of accelerated reluctance PEEC and MOR PEEC compare to a standard PEEC solver.

Parameter	Reluctance PEEC (spars.:94% to 98%)	Standard PEEC with MOR
Induced error	<1% to <7%	<1%
Solution time	3 to 5 times faster	~7 times faster
Memory usage	up to 25 times less	up to 200 times less

Macro model generation

Generating a macro model for use in higher level system simulations consist of creating an impedance matrix for the ports of interest and exporting it into a SPICE like format. Two methods exist:

First, is to simulate the impedance for one frequency of interest for each port, one by one, and collecting the self and mutual impedances into a matrix. The advantage of this method is that it results in a small sized matrix for fast

system level simulations. The drawback is that the impedance is theoretically valid for a single frequency only. In typical power electronic cases however, the inductance remains almost constant for a broad frequency range.

The second method (first published in [14]) is to first apply model order reduction to the PEEC matrix and then to directly export the reduced model to a SPICE like format. The advantage of this method is that it preserves the frequency dependency where the frequency bandwidth can be predetermined by the order of the model reduction. The drawback is that the model size is much larger and quickly increasing with number of ports and with complexity of the impedance characteristics (i.e. number of resonances).

The results of both methods are SPICE like sub-circuits that can be used in system-level simulations in combination with additional linear and non-linear circuit elements. Figure 12 shows the circuit used in this work to investigate the impact of the bus bar stray inductance on the overvoltages at turn-off. The time domain results are shown in Figure 13. Depending on the extraction frequency (1 Hz or 100 kHz), the simulated overvoltage peak slightly varies from 28 % to 34 %, representing a difference of about 20 % on the overvoltage design margins.

Figure 12: SPICE circuit with sub-circuit (yellow block) containing bus bar macro model.

Figure 13: Simulation results of IGBT turn-off transient, showing overvoltages for different bus bar macro models.

3D results

Solving the full PEEC model is much more time and memory consuming than applying model order reduction (see also Table 2). However, it preserves the full spatial information of the solution, thus allowing analyzing current density distributions (Figure 14) and magnetic field vector patterns (Figure 15).

Figure 14: Current density distribution.

Figure 15: Magnetic field pattern.

7. Conclusion

In this paper, we have presented a fast and efficient EM simulation methodology, which suits the model complexity of today's multilevel bus bars and circuits. The approach offers dedicated solving methods for different problem types. For 3D field solutions, it uses an accelerated (R, L_p)PEEC solver with a reluctance matrix approach and sparse direct solver, allowing for shorter computing time and less memory needs. For impedance extraction and macro model generation, it uses model order reduction techniques, allowing for fast frequency sweeps and frequency dependent, multi-terminal SPICE model generation. Reference measurements have been performed to demonstrate the accuracy over a broad frequency range. With this methodology, EM simulation of large complex bus bars and circuits is no longer a privilege of academic research; it has become an efficient design tool for competitive product development environments.

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