Impact of etch factor on characteristic impedance, crosstalk and board density

Abdelghani Renbi, Arash Risseh, Rikard Qvarnström and Jerker Delsing

*EISLAB, Department of Computer Science, Electrical and Space Engineering
Luleå University of Technology, SE-971 87 Luleå, Sweden*

*Abdelghani.Renbi@ltu.se, Arash.Risseh@ltu.se,
Rikard.Qvarnstrom@ltu.se and Jerker.Delsing@ltu.se*

Abstract

Signal integrity becomes more important when the length of the Printed Wiring Board (PWB) traces surpasses $\frac{\lambda}{10}$ where λ denotes the wavelength. For fast digital communication purpose and low energy consumption in CMOS technology, faster rise time of the clock which means higher harmonic frequency, has always been preferable. In this case, the importance of considering signal integrity gets a higher priority as issues such reflections and crosstalk between adjacent traces cannot be omitted, especially in dense High Density Interconnect (HDI) boards. Several factors control the effect of reflections and the crosstalk such as the shape and dimension of the traces, the isolator characteristics which is inserted between the trace and the ground plane, the nearness and the geometry of the nearby conductors. In other words, these factors control the characteristic impedance of the traces and the mutual inductances and capacitances between the adjacent traces. Although these factors have been taken into account during the design phase for good signal integrity, the manufacturing process, which differs from vendor to vendor, has a great impact on the above factors. PWB manufacturing process may result in many different variations, which involve the dielectric constant, the thickness of the insulator, the trace width and the copper foil thickness. In addition to these variations, the etching quality that falls mainly in three different categories of trapezoidal trace form. In this paper we present the effect of three different etching shapes on the characteristic impedance. Moreover, it is concluded that one could gain space which can be used for shrinking the electronics and/or saving the raw material when trading the characteristic impedance error for space. Similar method is followed to investigate the crosstalk reduction between two adjacent microstriplines when tolerating the error in the characteristic impedance. This procedure can only be applied when a 90° etch angle process is feasible.

Keywords: *Etch-factor, trace cross-section, crosstalk, characteristic impedance.*

1. Introduction

The industry keeps pushing towards smaller feature sizes and higher frequency signals in today's PWBs in order to make the devices smaller, faster and decrease the power consumption. Etching is one of the limiting factors in the conventional production process, both in terms of feature sizes and signal integrity. Previously the limitations in feature size and other technologies have been the main limitation factors. With recent improvements in circuit design and packaging, signal integrity and thereby impedance matching will become more of an issue.

PWB manufacturing starts with a base board

which consists of a substrate with a copper sheet on each side, only the top half is shown in figure 1a. Etch resist is applied to the top of the copper and exposed/cured through a mask using UV light, the unexposed parts are removed to reveal the copper that should be etched away, figure 1b. Halfway through the etch process the board will look like figure 1c, this shows that the edges of the trace have been exposed to the etchant which caused the round shape. The etch process is completed when the substrate can be seen between the traces, then it is just to remove the photoresist and the final board should look like figure 1d.

Fig. 1: Etching process steps

It is desired to get traces with rectangular cross section, this is currently not possible due to the etch process described above. This results in the underetching shapes seen in figure 2a, the "round" shapes are difficult to simulate and preform calculations on, so they are usually approximated by the trapezoidal shapes shown in figure 2b. For a normally etched trace which is the process target, the cross section equivalent can be approximated to a trapezoid with the same base width, height and 45° angles. The under etched trace might have slightly wider base since the etchant has not removed enough copper, this can be approximated to a trapezoid with 60° angles. If the board is over etched, too much copper will be removed and this can be approximated to a trapezoid with smaller angle, in this case 30°.

Fig. 2: (a) Etch shapes, (b) Etch equivalents.

The etch factor (F) is defined as the ratio between t and x in figure 3.

$$F = \frac{t}{x}$$

Fig. 3: Trace cross-section after etching.

One reason why rectangular cross sections are preferable, especially in RF-applications, is that one can be sure that the characteristic impedance of a transmission line matches the design. The shape of the trace cross section has influence on the inductance and the capacitance of the trace

which is larger in high frequency applications. A higher etch factor results in lower inductance and higher capacitance which bring the characteristic impedance of the trace closer to the theoretical value considered by board designers [1]. Another reason for making PWB with high etch factor is that traces with high etch factor can be made smaller than traces with low etch factor while keeping same impedance. This benefit will give a higher connectivity and results in better performance and in many cases, in lower manufacturing cost [2].

In high frequencies, smaller size microstriplines are more prone to mutual coupling which is well known as crosstalk due to close proximity to one another. Significant crosstalk might lead to false switching in digital circuits when it is not taken in consideration during the design phase. Crosstalk magnitude depends on line spacing, frequency or signal rise time, aggressor signal amplitude, line length and the geometry of the board and line.

In addition to low characteristic impedance error that can be achieved by a good etching process which leads to high etch factor, this paper calls the PWB research community to boost the focus on improving the etch factor. As mentioned before, an ideal etching process with 90° etch angle may contribute to smaller size and lower cost HDI boards when space and cost are the target interests. Some applications may seek to reduce the crosstalk as much as possible, employing an ideal etching process for the purpose will reduce a small amount of near-end cross talk. In this paper we present some simulation results of space and crosstalk reduction when using an ideal etching process instead of those which are illustrated in figure 2. These results apply to small size 50 Ω microstripline cases where FR-4 dielectric is employed as insulator.

2. Background

There are a few different main points that can be used to improve the circuit density of a board

1. Pads and vias,
2. Trace width,
3. Number of layers.

Reduction of the pad and via sizes will have a large benefit because large vias will block the signal path and will consume a lot of space especially for busses. Decreasing the trace width (and vias) might reduce the total amount of required layers, assuming the board size is fixed. Moreover, new layers could be added to the board in order to decrease the surface area, however this might have limited gain especially if a large amount of through hole vias are required. Vias and pads are limited in terms of connectivity and ability to drill exact holes because some margin is required. Thin-

ner copper foil which is required for etching small traces has adhesion issues due to the mechanical attachment to the dielectric. It also affects the high frequency performance in terms of crosstalk, noise and signal integrity. An increased number of layers makes the control of thermal and dielectric thickness more important. These methods will reduce the total amount of material and thereby the material cost [3].

There are many design rules involved when making a circuit board, trace width is the most relevant parameter for this research and how it affects the performance of the final board. Conventional HDI process limits the trace width to around 100 μm , smaller traces are possible but rapidly decreases yield [4].

3. Characteristic impedances error in different etching types

This section highlights the error in the characteristic impedance that is led by the etch angle in three etching types, it also emphasizes the significance of the impact that the etching process can have on the characteristic impedance. The characteristic impedance increases when the etch factor and trace width decrease. According to table II and figure 4 the deviations approaches 10 % when dealing with the smallest width and the worst etch angle. The computed error is relative to the illustrated characteristic impedance values in table I which correspond to 90° etch angle. These deviations might not be tolerated in some applications. In table II and others in the rest of the paper, the NA denotes the case where the etch angle is not applicable.

There exist small deviations from 50 Ω in the computed characteristic impedance values for the four widths in the case of 90° etch angle. The source of these deviations is that we kept the height of the insulator as a natural number in μm . On the other hand more computations have been iterated for the smallest possible error.

TABLE I: Characteristic impedance of pure rectangular microstripline in four typical trace widths when employing 4.5 dielectric constant FR-4 insulator and 18 μm copper thickness.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
90°	50.02	49.82	49.86	50

TABLE II: New characteristic impedance led by the imperfect etching in four typical trace widths.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
60°	50.9	51.84	50.6	52.89
45°	51.92	52.77	53.44	54.55
30°	52.9	53.52	54.79	NA

Fig. 4: Characteristic impedance error led by the imperfect etching in four typical trace widths.

4. Trading characteristic impedance error for space and raw material

Based on the characteristic impedance error, we already know that the characteristic impedance increases when the etch factor decreases. By decreasing the width of a rectangular trace we will be increasing the inductance per unit length L and decreasing the capacitance per unit length C thus increasing the characteristic impedance $Z_c = \sqrt{\frac{L}{C}}$. Let us assume that the etching process which leads to an infinite etch factor is feasible and we are satisfied by the trace characteristic impedance obtained by the imperfect etching process which is possible for non RF applications and those with electrically short lines. Under the previous assumption, one can trade this error of the characteristic impedance for space and raw material gain by going for pure rectangular traces but with smaller widths. Figure 5 describes the idea of achieving space gains which are noted by g_1 , g_2 and g_3 . In the normal case, we will etch for the case in figure 5 (a) and we will achieve an exact characteristic impedance without positive deviation. If we can tolerate a small increase in the characteristic impedance, one can go for case (b) where the characteristic impedance is equal to the one that is achieved by the under etching when the etch angle is equal to 60°. Tolerating more the error of the characteristic impedance, we will reduce the rectangular trace even further as shown in figure 5 (c), until we reach the characteristic impedance that corresponds to the 45° trapezoidal trace, the best gain is achieved when we tolerate the characteristic impedance to the one that corresponds to in 30° trapezoidal trace.

Table III and figure 6 illustrate the space gain that can be achieved when applying the idea for

Fig. 5: Basic idea of reducing space and raw material.

four different width capabilities. The gain figures are the simulation results for 50 Ω microstriplines on a FR-4 insulator with 4.5 dielectric constant. Fundamentally, the gain is larger when tolerating the characteristic impedance obtained by the worst etching process.

TABLE III: Space gain in (μm) when perfect rectangular traces replace trapezoidal traces but keeping the same characteristic impedance.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
90°	0	0	0	0
60°	6	9	2	5
45°	13	13	11	8
30°	17	16	13	NA

Fig. 6: Space gain in (μm) when perfect rectangular traces replace trapezoidal traces but keeping the same characteristic impedance.

Now it is up to the initial purpose of gaining space, which can be either shrinking the electronics and/or reducing raw material and process costs. Tables IV and V summarize the gains in (trace %) for 100 μm and 50 μm spacing capabilities, the smaller spacing capability the better trace gain will be achieved which puts the technology with low spacing capability in better position for benefiting from the idea. The gained space includes the nominal spacing between the traces and may be used for extra traces or other components. In addition to smaller size feature, one can reduce process and raw material costs by exploiting the gained space for traces from other layer and hopefully getting rid of the necessity of building an extra layer in the board which translates in process and raw material costs.

TABLE IV: Gain in (trace %) when perfect rectangular traces replace trapezoidal traces but keeping the same characteristic impedance, in case of 100 μm spacing.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
90°	0	0	0	0
60°	2.04	3.73	1.01	3.45
45°	4.53	5.49	5.82	5.63
30°	6.01	6.84	6.95	NA

TABLE V: Gain in (trace %) when perfect rectangular traces replace trapezoidal traces but keeping the same characteristic impedance, in case of 50 μm spacing.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
90°	0	0	0	0
60°	2.46	4.71	1.35	5.26
45°	5.49	6.95	7.91	8.7
30°	7.3	8.7	9.49	NA

5. Trading characteristic impedance error for better crosstalk

Crosstalk prediction and reduction have always been two essential topics to design for reliable high speed and dense electronics. One of the most popular techniques which reduces the crosstalk is to use a guard trace between the victim and the aggressor lines, the guard trace which is grounded at two or more points along its length will shield the traces it lies between [5], on the other hand the guard trace method does not help for low cost and dense electronics. Another interesting technique which is published in [6], suggests to use asymmetric stub loaded lines, the method significantly reduces the near-end and far-end crosstalk, however implementing stubs between traces for extremely small spacing such 100 μm and 50 μm might very hard with the current manufacturing process.

According to [7], increasing $\frac{S}{W}$ must lead to near-end and far-end crosstalk reductions, where S is the spacing between the traces and W is the width of the traces. In this section we will present some simulation results of the crosstalk reduction when applying the assumption which is described in section 4. Instead of employing gained space for improving board density, this time we use the gained space to increase the proximity of the traces. Figure 7 shows four cases, where (a) is the original case of the perfect etching process without characteristic impedance error and with S spacing between the traces, (b) is the case where we tolerate the characteristic impedance error of

60° trapezoidal trace in perfect rectangular traces and therefore the spacing becomes $S + d_1$ where d_1 satisfies the condition of keeping the center of the traces at the same X position. This applies similarly to case (c) and (d) which correspond to 45° and 30° trapezoidal microstriplines.

Fig. 7: Basic idea of reducing the crosstalk.

Increasing the spacing S is one way to reduce the mutual coupling, in this case we do increase the spacing between the traces, but the trace width is also minimized in order to keep the same board density as 90° etch angle. Tables VI and VII illustrates the reduction in the near-end crosstalk S_{31} for four typical widths and two spacing capabilities. Although it is not significant but it might be worthwhile to take into consideration in some applications. According to figure 8 and 9, the crosstalk reduction is almost constant between 1 cm and 5 cm length of the coupled lines.

TABLE VI: Crosstalk reduction in (dB) when perfect rectangular traces replace trapezoidal traces but keeping the same characteristic impedance, in case of 100 μm spacing.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
90°	0	0	0	0
60°	0.21	0.55	0.33	0.43
45°	0.64	0.78	0.67	0.76
30°	0.89	0.95	0.08	NA

TABLE VII: Crosstalk reduction in (dB) when perfect rectangular traces replace trapezoidal traces but keeping the same characteristic impedance, in case of 50 μm spacing.

Etch angle	Trace width			
	200 μm	150 μm	100 μm	50 μm
90°	0	0	0	0
60°	0.39	0.64	0.21	0.24
45°	0.85	0.96	0.94	0.5
30°	1.07	1.19	1.11	NA

Fig. 8: S_{31} plot of the four etch cases for 150 μm width, 50 μm spacing and 5 cm trace.

Fig. 9: S_{31} plot of the four etch cases for 150 μm width, 50 μm spacing and 1 cm trace.

6. Conclusion

This work shows that the etch angle has a significant impact on the characteristic impedance. Trading the characteristic impedance error for space and raw material when a 90° etch angle process is feasible, could be beneficial for high production volumes and can be a cost saving source if it results in reduced number of layers in HDI boards. Employing similar idea and trading characteristic impedance error for crosstalk reductions lead to a small improvement which can be beneficial in applications where crosstalk reduction has a high priority.

References

- [1] S. Monroe and O. Buhler, "The effect of etch factor on printed wiring characteristic impedance." IEEE EMC Society, 2001.
- [2] C. F. Coombs, *Printed Circuits Handbook*, 6th ed. McGraw-Hill Professional Publishing, 2007, ch. 2 - Electronic Packaging and High-Density Interconnectivity, pp. 2.16–2.21.
- [3] —, *Printed Circuits Handbook*, 6th ed. McGraw-Hill Professional Publishing, 2007, ch. 9 - Base Materials Performance Issues, pp. 9.1–9.7.
- [4] —, *Printed Circuits Handbook*, 6th ed. McGraw-Hill Professional Publishing, 2007, ch. 22 - Introduction to High-Density Interconnection (HDI) Technology, pp. 22.3–22.11.
- [5] D. Ladd, "Spice simulation used to characterize the cross-talk reduction effect of additional tracks grounded with vias on printed circuit boards," *IEEE Transactions on*, 1992.
- [6] S.-K. Koo and H.-S. Lee, "Crosstalk reduction effect of asymmetric stub loaded lines," *J. of Electromagn. Waves and Appl*, 2011.
- [7] Y.-S. Sohn, "Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board," *IEEE Transactions on*, 2001.