PROXIMITY EFFECTS OF "UNUSED" OUTPUT BUFFERS ON ESD PERFORMANCE

J.P. LeBlanc and M.D. Chaine
Texas Instruments Incorporated
M/S 681 P.O. Box 1443
Houston, Texas 77001

ABSTRACT

A unique failure mechanism, identified on an "unused" output buffer located near a used input protection device, occurs when excessive substrate current is generated during an ESD event. This ESD failure mechanism, dubbed the "proximity effect," has been demonstrated on a variety of I/O buffer layouts, and a solution has been identified.

I. INTRODUCTION

The design of ESD protection circuitry for advanced VLSI devices has recently become more challenging. This is especially true for integrated circuits developed in submicron CMOS technology with pumped substrate. With the increase in the number of input and output pins on a device, the interaction of their respective ESD protection circuitry potentially can generate ESD failures.

When the MIL-STD-883C was changed in March 1989, the new method 3015.7 changed the pin combinations to be tested. One of the new combinations is to ESD stress all input and output pins, both positive and negative, with respect to the power supply, V_{cc}.

Recent ESD testing using this new pin combination on memory arrays has demonstrated a unique ESD failure mechanism. These arrays are option programmable by using a different metal mask during fabrication. Some of the metal mask options have "unused" output buffers located near "used" ESD input protection circuitry. During an ESD event, failures occur when substrate current is generated between the ESD protection circuitry and the "unused" pull-up transistor buffer connected to V_{cc}. This new mechanism, dubbed the "proximity effect," plays an important role when the n moat region of an input ESD circuit is within 20 microns from an unrelated n moat diffusion region contacted to V_{cc}.

The purpose of this paper is to report how this failure mechanism was discovered and how it operates. This paper describes the most common ESD input protection circuitry and how it functions when stressed with respect to V_{cc}. This is followed by a specific example illustrating the "proximity effect" failure mechanism and its operation.

II. INPUT PINS STRESSED WITH RESPECT TO V_{cc}

The basic input ESD protection circuit configuration consists of a primary protection device, a resistor, and a secondary device. When activated the primary protection device, typically a thickfield device, an SCR, or a large p-n diode, shunts the majority of the high currents away from the sensitive internal circuits during an ESD event. The secondary protection device, a field plate diode, a thick field device, or a p-n diode, limits the voltage across the first gate oxide. Finally, the resistor reduces the current that reaches the secondary device, as well as helping to trigger the primary device. [1]

With recent changes in CMOS technology to improve reliability and performance, the trend has been to use lateral SCR (LSCR) devices instead of thick-field devices for the primary protection device [2]. This has been especially true when graded junctions or lightly doped drain (LDD) transistors with/without silicided diffusions are used. Also, field-plate diodes have frequently been used as the secondary protection device [3].

As shown in Figure 1, the complete input protection curcuit consists of an LSCR, an n moat diffusion resistor, and a field plate diode (FPD). The operation of the LSCR during an ESD event is reported in reference 2. The typical trigger voltage range of the LSCR for a 1.0-μm CMOS technology can vary from 50 to 70 V; consequently, the FPD/resistor combination must be designed to withstand this ESD stress. [3]

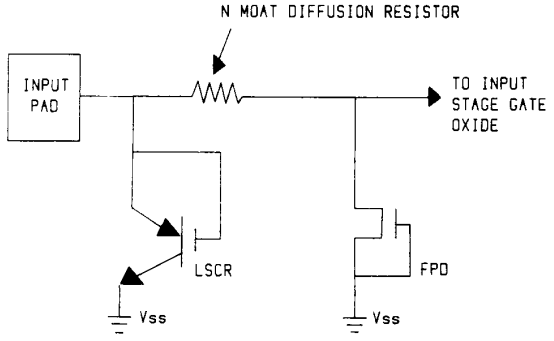

Figure 1. Input ESD Protection Circuitry [3].

When the input pad in Figure 1 is stressed positive with respect to V_{cc}, the FPD clamps the voltage and protects the first input stage gate oxide while operating in the snap back mode of the lateral npn transistor. The voltage drop across the n moat diffusion resistor increases until the voltage at the pad is sufficient to trigger the LSCR (See Figure 2). [1,2]

The voltage along the floating V_{ss} bus is held positive with respect to V_{cc} causing the forward biasing of internal diodes connected between the V_{cc} and V_{ss} buses. After the LSCR triggers, the ESD current has a direct path to V_{cc} and the rest of the circuit is protected from the ESD stress. [4,5]

The operation of this type of input ESD protection circuit when a negative stress is applied to the pad while V_{cc} is grounded is more complex. The function of each element of the protection circuitry changes because the p-n junction that exists between the p substrate and the n moat region in each device (the n moat resistor, the FPD and the LSCR) becomes

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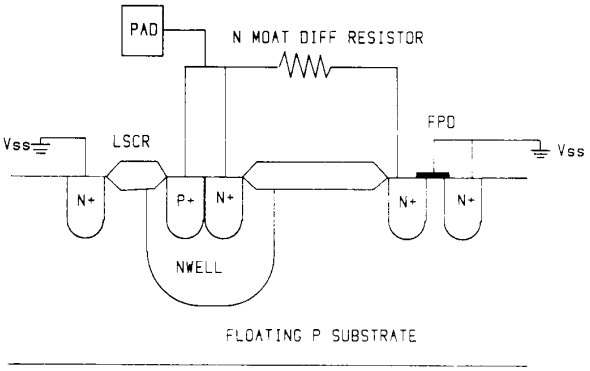

Figure 2. Profile of LSCR and FPD Devices [3].

forward biased. Consequently, the input ESD protection circuitry behaves more like a very large resistive diode network.

During the negative pulsed event, the input ESD protection circuit injects a large amount of negative current into the substrate, which forces the voltage on the substrate with respect to V_{cc} to become more negative. This effect increases the reverse bias voltage on all of the p-n junctions contacted to V_{cc}. Those V_{cc} moat and n well regions nearest the ESD input protection circuit experience the highest reverse biased stress. Eventually, the ESD event injects enough holes and electrons into the substrate to cause current to flow from the V_{cc} bus through the reverse biased junctions, through the substrate, and through the forward biased diodes of the input ESD protection curcuitry (See Figure 3).

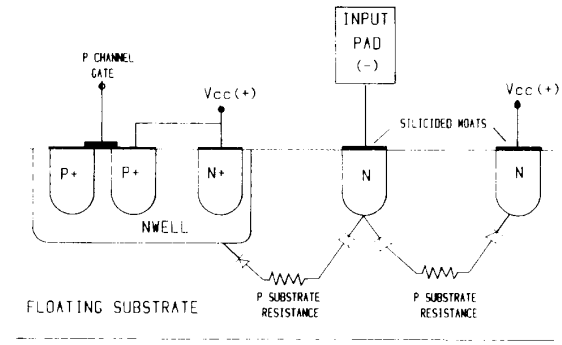

Figure 3. Current Flow from the V_{cc} Moats to the Input PAD.

III. ESD TEST RESULTS

During extensive HBM ESD testing on a memory array with mask programmable device options, consistent standby current (ICC2) failures occurred when the stress was applied negative with respect to V_{cc}. The voltage required to induce these substrate leakage failures ranged from -2.0 to -2.5 Kv.

The ESD testing was performed on a commercially available multi-port automatic tester. This tester has the capability to systematically test each pin combination required by the MIL STANDARD HBM ESD test. In addition, both junction breakdown voltages and leakage currents were measured by this tester before and after each pin was stressed.

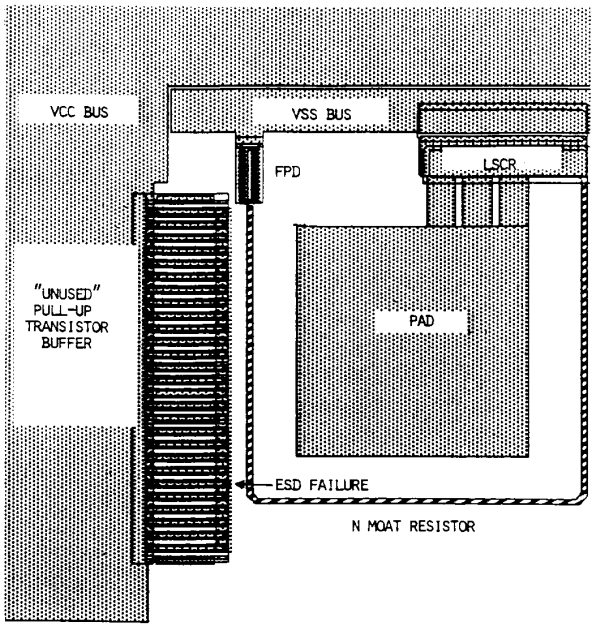

Figure 4. "Unused" Pull-up Transistor Buffer and Input Protection Circuitry.

With the support of our failure analysis laboratory, the location of the V_{cc} substrate leakage was isolated. Additional ESD tests confirmed that the failure happened only during the negative stress and not during the positive stress.

Since this IC is programmable using different metal mask options, some of the pins can function as input or as output pins depending on which metal mask has been selected. As a result, both input ESD circuitry and output pull-up and pull-down buffers have been designed around these pins.

The failure that was identified occurred at the end of a transistor finger connected to V_{cc} on an "unused" pull-up output buffer located near a "used" input ESD protection circuit. In Figure 4 an illustration shows the "unused" pull-up transistor buffer, the FPD, the n moat diffusion resistor, and the LSCR. An arrow points to the location where the substrate leakage was found (See Figures 4 & 5).

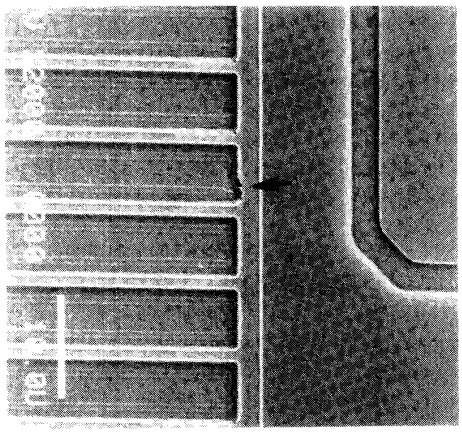

Figure 5. N Moat Resistor and Damaged V_{cc} Transistor Finger.

In Figure 6 the transistor finger contacted to V_{cc} shows extensive p-n junction damage. The secondary effect of thermal heating of the junction has caused breakdowns to appear in both the oxide and the poly layers.

As discussed in Section II, when the input pin is stressed negative with respect to V_{cc}, the injection of electrons from the input ESD protection circuit forces the substrate voltage negative with respect to V_{cc}. This negative voltage causes the reverse bias of all of the p-n junctions between the n moat transistor figures and the p substrate. The junction damage at the end of the finger shown in Figure 6 is caused by excessive electron avalanche current generated between the n moat of the finger and the n moat of the resistor. Additional junction damage at the end of the other fingers is not observed because the first finger becomes the least resistive path and protects the other fingers from junction breakdown damage.

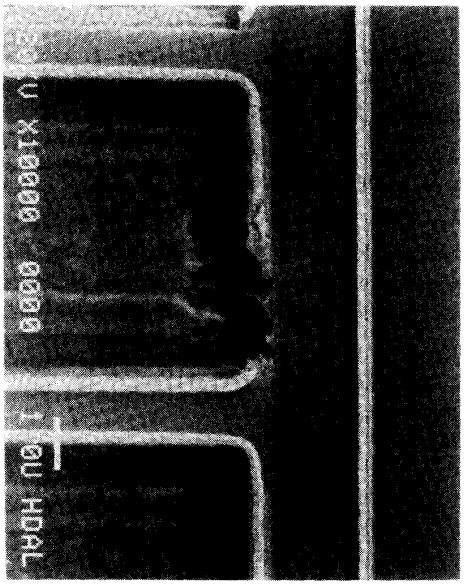

Figure 6. P-N Junction Damage at the end of the Finger.

IV. PROXIMITY EFFECT

The ESD failure described above occurs when unrelated n moat to n moat distances are within 20 microns. At these short distances, the substrate resistance is now low enough for excessive substrate currents to flow between the n moats and damage the reverse biased n moat/substrate junction. This ESD failure mechanism has been dubbed the "proximity effect."

As the voltage between the n moat resistor and the V_{cc} moat region increases, current generated from the forward bias n moat resistor will flow towards the V_{cc} n moat. Because of the relatively large distance between the n moat regions, the parasitic lateral npn transistor acts like a forward biased diode, a resistor, and a reverse biased diode. Consequently, this parasitic transistor does not turn on. If the voltage across the reverse biased junction at the end of the transistor finger is high enough, avalanche currents will be induced. When this occurs the current can increase dramatically, causing excessive heating of the p-n junction. Damage to the junction will quickly follow, resulting in excessive ICC2 leakage to the substrate during electrical endpoint testing.

Some of the critical parameters that determine the ESD breakdown voltage involved in the "proximity effect" are the distances between the n moats, the resistivity of the substrate, and the type of n moat regions involved. The exact relationship of these parameters to the ESD breakdown voltage is not fully understood at this time. Additional ESD studies need to be completed before a specific relationship can be developed.

Another factor that may affect this mechanism would be the use of a grounded substrate. More ESD studies need to be done to determine if this failure mechanism exists when the substrate is grounded. The devices analyzed in this work used an ungrounded substrate.

V. LASER CUT EXPERIMENT AND DESIGN CHANGES

As discussed in Section IV, the distance between the input n moat resistor and the V_{cc} n moat region is one of the critical parameters that affects the ESD breakdown threshold voltage. If this distance is expanded, the substrate resistance would increase thereby improving the ESD failure threshold voltage. Consequently, if the V_{cc} bus contacted to the n moat region of the "unused" pull-up transistor buffer is removed, there would be no substrate resistance path, and this failure mechanism would be eliminated. A laser cut experiment was performed on this IC device to test this theory.

The experiment consisted of two sets of three units. The first set of units had the "unused" pull-up output buffer electrically disconnected by laser cutting the metal from the V_{cc} bus. The second set of units had the top of the plastic and polyimide protective layer removed like the first set, but the "unused" pull-up output buffer was not disconnected. These units were used as control units. Both sets of units had the input pin ESD stressed both positive and negative with respect to V_{cc}. The test results are shown in Table 1.

TABLE 1.

LASER CUT ESD TEST RESULTS

LASER CUT UNITS	INPUT PIN	V_{cc} PIN	TEST RESULTS	MAXIMUM STRESS VOLTAGE APPLIED
1,2,3	POSITIVE	GROUND	PASSED	+6.0KV
	NEGATIVE	GROUND	PASSED	-6.0KV
CONTROL UNITS				
1	POSITIVE	GROUND	PASSED	+3.5KV
	NEGATIVE	GROUND	FAILED	-3.5KV
2	POSITIVE	GROUND	PASSED	+2.5KV
	NEGATIVE	GROUND	FAILED	-2.5KV
3	POSITIVE	GROUND	PASSED	+2.5KV
	NEGATIVE	GROUND	FAILED	-2.5KV

Based on the results of this experiment, a new metal mask was designed that disconnected the V_{cc} bus from this "unused" pull-up output buffer. Again, ESD tests were performed testing this input pin with respect to V_{cc}. The test results were the same as the laser cut experiment. The units passed both the positive and negative ESD stress pulses up to 6.0 Kv!

VI. CONCLUSION

Recent ESD testing on an IC developed in submicron CMOS technology using the MIL-STD-883C, method 3015.7, has revealed a new ESD failure mechanism, called the "proximity effect". This mechanism can potentially occur when input pins are stressed negative with respect to V_{cc}. This paper has reviewed the operation of the most commonly used ESD input protection circuitry when stressed with respect to V_{cc}. The failure mechanism that accounts for this type of ESD failure has been discussed. A laser cut experiment has verified that disconnecting the V_{cc} bus from the "unused" n moats eliminates this type of ESD failure. Device metal mask changes have confirmed these findings.

The proximity effect has been discovered to play a significant role in ESD protection capability. The best solution to eliminate this type of ESD failure is to develop better design and layout rules that will prohibit the layout of n moat regions contacted to V_{cc} near the input ESD circuitry. From our ESD test results, we know that an "unused" n moat region contacted to V_{cc} within 20 μm of an input ESD protection circuit will be damaged, and that the ESD failure threshold will occur below 3.0 Kv. Additional ESD studies need to be performed to determine the exact spacial relationship between the two different n moat regions and to examine if this type of failure mechanism exists when the substrate is grounded.

VII. ACKNOWLEDGEMENTS

The authors would like to thank the excellent failure analysis work performed by Dr. Seshu Pabbisetty's (Texas Instruments) Houston Device Analysis Laboratory. We would also like to thank Mr. Bob Rountree and Dr. Charvaka Duvvury for their valuable discussions, and Mr. Bret Reed for taking the ESD data.

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