Time Stretcher for a Time-to-Digital Converter with a Precisely Matched Current Mirror

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Abstract—This paper presents an approach for the design of a time stretcher based on charging and discharging a capacitor by currents with a ratio equal to the desired stretch factor. The stretched time interval can be measured by using a time-to-digital converter to achieve improved system resolution. Expressions for the current source output impedance and transistor area required to reach a specified linearity and matching are derived. The realization uses wide-swing current mirrors to achieve the required output impedance at an acceptable voltage swing at the capacitor. The derived expressions and the overall design are validated with schematic and extracted simulations in a 0.35 μm CMOS process technology.

Keywords: Time-to-digital converter, time stretcher, stretch factor, current mirror, analogue time expansion, comparator.

I. INTRODUCTION

The performances of time-to-digital converters are mainly determined with finite SNRs (signal-to-noise ratios) and mismatching of integrated elements [1]. Measuring time with picoseconds-level resolution is a tremendous challenge. To minimize the impact of finite SNRs and mismatching of integrated elements, the concept of time stretching or analogue time expansion can be an effective solution. Time stretching processes small time difference and outputs a larger time difference as shown in Fig. 1, which can improve the resolution of time-to-digital converters. The complete architecture of the time-to-digital converter design is presented in [2]. This time-to-digital converter can be implemented as an integrated circuit for a 3D time-of-flight camera, where it will be embedded on a sighted wheel chair [3] for 3D mapping and obstacle navigation.

In this work, an analogue time stretcher with a stretch factor is designed from standard building blocks, such as current mirrors. The most significant features for determining the feasibility and performance of the current mirror are the following: acceptable accuracy, high output impedance, high linearity and small area [4] [5] [6]. This work is divided into seven sections. Section II presents a current mirror-based time stretcher. In section III, the design constraints are discussed in detail. In sections IV and V, we focus on the practical design, layout and simulations. The results are presented in section VI. Section VII briefly describes about the layout strategy. This work is concluded in section VIII.

Fig. 1. Architecture of TDC based on time stretcher.

II. A CURRENT MIRROR-BASED TIME STRETCHER

In analogue time expansion [7] [8], the time interval to be measured is stretched by a factor k , realized by charging a capacitor with a constant current I , followed by discharging the capacitor by a constant current $\frac{I}{k}$. This stretched time interval can be measured with a time-to-digital converter with a lower resolution [7].

The design consists of a current mirror, current source and precisely matched current sinks and dummy elements. Constant current $\frac{I}{k}$ is produced in the current sink and is copied in similar current sinks to achieve an appropriate stretch factor. Dummy elements are added to provide identical temperature gradients and similar boundary conditions. The operating principle of the current mirror-based time stretcher is shown in Fig. 2. During an idle state, the *nmos* switch conducts and V_{out} is zero. *Start* opens the *nmos* switch and thereby removes a short circuit across the capacitor. The voltage across the capacitor increases linearly until the rising edge of the *Stop* signal. The resulting voltage across the capacitor is a linear ramp that is directly proportional to time t : $V_{out}(t) = I_1 * t / C_{conv}$, where C_{conv} is the conversion capacitance and I denotes the constant charging current. After the arrival of the *Stop* signal, the conversion capacitor is isolated, and the voltage across the capacitor remains constant. A current sink with *nmos* transistors is used to initiate capacitor discharging with $\frac{I}{k}$, a fraction of the charging current. Using this design technique, the constant current I is an exact copy of $\frac{I}{k}$, but with a stretch factor k , and thus achieves an analogue

Fig. 2. Time stretcher schematic.

time expansion that may be used to improve the time-to-digital conversion resolution [7] [8]. The current mirror-based time stretcher schematic circuit with stretch factor $k=4$ is shown in Fig. 2.

III. DESIGN CONSTRAINTS

A. Current mirror matching

The time stretcher design challenge is a trade-off between complexity, current mirror matching, area and low power consumption, considering the constraints for a particular application. Additionally, precise stretch factor matching is required [9]. If the current mirrors are not precisely matched, the design may suffer from gain error. An estimation has been performed based on the Pelgrom's MOS transistor-mismatching model devices to determine the relationship between area and mismatching [13]. The threshold voltage mismatch can be written as

$$\sigma \Delta V_{th} = \frac{A_{VT}}{\sqrt{WL}}. \quad (1)$$

The conductance parameter mismatch can be written as

$$\sigma \frac{\Delta \beta}{\beta} = \frac{A_{\beta}}{\sqrt{WL}}. \quad (2)$$

Considering the standard deviation of the drain source model that is valid in all regions of operation, we can write

$$\sigma \frac{\Delta I_D}{I_D} = \sqrt{\left(\frac{\sigma \Delta \beta}{\beta}\right)^2 + \left(\frac{g_m}{I_D}\right)^2 (\Delta V_{th})^2}. \quad (3)$$

TABLE I. REQUIREMENTS SET FOR DESIGN CONSTRAINTS

Parameter	By analysis
Current mirror matching ($\sigma(\frac{\Delta I_{DS}}{I_{DS}})$)	1%
Overdrive Voltage (V_{ov})	300 mV
V_{error} from full voltage swing	1% of 2 V
Linear dynamic range	70 ns $\approx$ 12 meters
$\frac{kT}{C}$ (Capacitor noise)	50 fF $\leftrightarrow$ 0.029 mV
Output Impedance	$\approx$ 25 M Ω

This equation can further be simplified to identify an appropriate MOS transistor channel length as:

$$\left(\sigma \frac{\Delta I_D}{I_D}\right) = \sqrt{\frac{A_{\beta}^2}{(WL)} + \left(\left(\frac{2I_D}{V_{ov}}\right)\left(\frac{1}{I_D}\right)\left(\frac{A_{VT}}{\sqrt{WL}}\right)\right)^2}, \quad (4)$$

$$\left(\sigma \frac{\Delta I_D}{I_D}\right) = \frac{1}{\sqrt{WL}} \sqrt{A_{\beta}^2 + \left(\frac{2}{V_{ov}} \times A_{VT}\right)^2}, \quad (5)$$

$$\sqrt{WL} = \left(\sigma \frac{\Delta I_D}{I_D}\right) \sqrt{A_{\beta}^2 + \left(\frac{2}{V_{ov}} \times A_{VT}\right)^2}. \quad (6)$$

Additionally $\frac{W}{L}$ for all devices can be calculated using the drain current as shown in this equation

$$\frac{W}{L} = \frac{2I_D}{\mu_{n,p} C_{ox} V_{ov}^2}. \quad (7)$$

B. Required linearity and output impedance

The required output impedance is directly related to the integral non-linearity. In our design, this non-linearity is translated into error in respective time and distance measurements. With the proposed circuit design, a numerical evaluation was performed regarding the required output impedance as a function of linearity.

The time stretcher can be modeled as a simple RC circuit, as shown in Fig. 3(a), with a current source, resistance R and a capacitance C , having an initial voltage V_0 . We can write

$$\frac{dV}{dt} = -\frac{V}{CR} - \frac{I}{C}, \quad (8)$$

and the voltage across the capacitor can be derived as a function of time with

$$V_t = (V_0 + IR) \times e^{-\frac{t}{RC}} - IR. \quad (9)$$

Fig. 3. Time Stretcher modelled as RC circuit.

In Fig. 3, V_{ref} represents an ideal ramp voltage between extreme points t_{min} and t_{max} . The integral non-linearity can be defined as the maximum deviation of the actual transfer characteristic from a straight line, where the line is

$$V_{ref}(t) = (V_{tmax} - V_{tmin}) \times \frac{t_{min}}{t_{max} - t_{min}} + V_{tmin}. \quad (10)$$

From Fig. 3, the integral non-linearity V_{error} can be written as the maximum deviation from V_{ref} as a function of time,

$$V_{error} = \max(V_t - V_{ref}(t)). \quad (11)$$

Combining equations 9 and 10, we can write

$$V_{error} = \max | (V_0 + IR) \times e^{\frac{-t}{RC}} - IR - (V_0 + IR) \times (e^{\frac{-t_{max}}{RC}} - 1) \times \frac{t}{t_{max}} - V_0 |, \quad (12)$$

$$V_{error} = \max | (V_0 + IR) \times \overbrace{\left(e^{\frac{-t}{RC}} - \frac{t}{t_{max}} \times (e^{\frac{-t_{max}}{RC}} - 1) - 1 \right)}^A |. \quad (13)$$

Solving A to evaluate t at the point of maximum error,

$$\frac{dA}{dt} = \frac{1}{RC} \times e^{\frac{-t}{RC}} - \frac{1}{t_{max}} \times (e^{\frac{-t_{max}}{RC}} - 1), \quad (14)$$

and solving for t,

$$e^{\frac{-t}{RC}} = -\frac{RC}{t_{max}} \times (e^{\frac{-t_{max}}{RC}} - 1); \quad (15)$$

Thus,

$$t = -RC \ln\left(\frac{RC}{t_{max}} \times (1 - e^{\frac{-t_{max}}{RC}})\right). \quad (16)$$

Expanding eq. 12 using Taylor's expansion

$$t = -RC \times \ln\left(1 - 1 + \frac{t_{max}}{RC} - \left(\frac{t_{max}}{RC}\right)^2 \frac{1}{2}\right), \quad (17)$$

$$t \approx -RC \times \ln\left(\frac{RC}{t_{max}} \times \left(\frac{t_{max}}{RC} - \left(\frac{t_{max}}{RC}\right)^2 \frac{1}{2}\right)\right), \quad (18)$$

$$t \approx -RC \times \ln\left(1 - \frac{t_{max}}{RC} \times \frac{1}{2}\right), \quad (19)$$

$$t \approx -RC(-) \times \ln\left(\frac{t_{max}}{2RC}\right). \quad (20)$$

Assuming $t \ll RC$, we find t for the maximum error as

$$t \approx \left(\frac{t_{max}}{2}\right). \quad (21)$$

Using eq. 12 and eq. 21, the following simplifies to:

$$V_{error} = (V_0 + IR) \times \left(e^{\frac{-t_{max}}{2RC}} - \frac{1}{2} \left(e^{\frac{-t_{max}}{RC}} - 1\right) - 1\right), \quad (22)$$

thus

$$V_{error} = (V_0 + IR) \times \left(e^{\frac{-t_{max}}{2RC}} - \frac{1}{2} e^{\frac{-t_{max}}{2RC}} - \frac{1}{2}\right). \quad (23)$$

Expanding D using Taylor's expansion, we can obtain an expression for V_{error} , which can be further simplified to achieve an approximate value for the required linearity output impedance:

$$D \approx \frac{1}{8} \left(\frac{t_{max}}{RC}\right)^2 - \frac{1}{4} \left(\frac{t_{max}}{RC}\right)^2 = -\frac{1}{8} \left(\frac{t_{max}}{RC}\right)^2. \quad (24)$$

Thus,

$$V_{error} = \frac{IR}{8} \left(\frac{t_{max}}{RC}\right)^2 = \frac{I}{8C^2} \times t_{max}^2 \left(\frac{1}{R}\right), \quad (25)$$

solving for R yields the required output impedance,

$$R = \frac{I}{8} \left(\frac{t_{max}}{C}\right)^2 \left(\frac{1}{V_{error}}\right). \quad (26)$$

C. Conclusion from design constraints

Table 1 presents the system-level design requirements to be used in determining our required design specifications. In section III.(A) A_{VT} , A_β and μC_{ox} represents constants that are technology dependent. The value of $\sigma(\frac{\Delta I_{DS}}{I_{DS}})$ has been assumed to be 1%. In section III.(B), the output impedance was calculated assuming a $V_{error} = 1\%$ of 2 V (output voltage swing). For this work, we used a charging current of $I = 2\mu A$ and a capacitance of $C = 50 fF$. The $\frac{kT}{C}$ noise associated with the capacitor was 0.029 mV rms, which corresponds to a fraction of centimeter in distance error. t_{max} represents the dynamic range of the time stretcher, with a design value of 70 ns ≈ 12 meters in distance measurement.

Based on the design requirements, equations (6), (7) and (26) were evaluated to determine the required output impedance and device sizing for matching. The output

TABLE II. DESIGN SPECIFICATIONS

Parameter	Proposed Structure#1
PMOS ($\frac{W_2}{L_2} = \frac{W_3}{L_3}$)	1500nm / 3200nm
PMOS ($\frac{W_1}{L_1} = \frac{W_4}{L_4}$)	1500nm / 1500nm
NMOS ($\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_4}{L_4}$)	1500nm / 4000nm
VDD	3.3V
No Of Transistors	5

Fig. 4. High swing cascode current mirror architecture (a) High swing cascode current source (b) High swing cascode current sink.

impedance evaluated during capacitor charging was $25 \text{ M}\Omega$. The output impedance for discharging is k times that required for charging. The transistors $\sqrt{WL}$, as evaluated with derived equations (6) and (7) are $\approx 2.5 \text{ }\mu\text{m}$ and $\approx 3 \text{ }\mu\text{m}$, for *nmos* and *pmos*, respectively. The final device sizes used for the design are listed in Table 2.

IV. THE HIGH SWING CASCODE CURRENT MIRROR

A high swing cascode current mirror is the preferred topology for the proposed time stretcher (Fig. 4), due to its low voltage operation, capability of output voltage swing, simplicity, small area and reasonable degree of precision [10] [11]. The circuit is characterized by its moderately low input impedance $R_{in} = \frac{1}{gm_4}$ ($\sim k\Omega$) and moderately high output impedance $R_{out} = r_{o1}g_{m2}r_{o2}$ ($\sim M\Omega$) [10]. The notations: r_o and g_m represent MOS transistor small-signal output resistance and transconductance respectively, where r_{o1} represents the source/sink and r_{o2} presents the small-signal output resistance for cascodes.

Fig. 4(a) demonstrates the high swing cascode current source based on *pmos* transistors used for charging the capacitor with constant current. The main current source devices are Mp1 and Mp3, with Mp2 and Mp4 acting as cascode devices and Mp5 as a biasing transistor that sets the desired V_{DS} , by ensuring that the rest of the devices remain in saturation. The value for V_{OV} was chosen based on the required linear output voltage swing for the time stretcher. The main current source devices Mp1 and Mp3 must be precisely matched to achieve the low output current variation specified for the source current. As the current varies inversely with transistor channel length, the channel length of transistors Mp1 and Mp3 were high, as presented in section III. The typical V_{OV} for the current sources Mp1 to Mp4 and current sinks Mn1 to Mn4 were chosen as 300 mV and 350 mV, respectively. The values for V_{OV} were selected as a compromise with respect to the required output voltage swing and high output impedance for the time stretcher. In this design, $I_{ref,pmos} \approx 2 \text{ }\mu\text{A}$ for the *pmos*-based current source and for the *nmos*-based current mirror with $k=4$ $I_{ref,nmos} = I_{ref,pmos}/4 = 0.5 \text{ }\mu\text{A}$ were selected (Fig.2).

The current sinks are implemented using *nmos* transistors for capacitor discharging and mirroring, as shown in Fig. 4

Fig. 5. Output current in terms of output voltage (*pmos*).

Fig. 6. Output current in terms of output voltage (*nmos*).

(b). As previously discussed, the channel lengths of the main current source devices Mn1 and Mn3, presented in section III are high to minimize mismatches. In both cases, the cascode device mismatches do not significantly contribute to the output current matching. Although not applied here, the channel length of the cascode devices could be smaller as a trade-off to save area and to minimize the output capacitance at the output of current source and sink outputs.

V. IMPLEMENTATION

The proposed high swing cascode current mirror-based time stretcher was designed and simulated in a $0.35 \text{ }\mu\text{m}$ CMOS process. The design was implemented for stretch factor $k=4$, $k=9$, $k=14$ and $k=19$, to understand the influence of the parasitics and possible trade-off between time stretcher area and resolution for time-to-digital converter. The mismatch due to random variations is kept at a manageable level by using appropriate device sizing as derived in section (III). A common centroid layout technique for the current mirrors was used in order to minimize the impact of systematic errors [12]. A time stretcher with $k=4$ occupies an area of $24 \times 32 \text{ }\mu\text{m}^2$, $k=9$ occupies an area of $52 \times 46 \text{ }\mu\text{m}^2$, $k=14$ occupies an area of $67 \times 47 \text{ }\mu\text{m}^2$ and $k=19$ occupies an area of $78 \times 48 \text{ }\mu\text{m}^2$, respectively.

Fig. 7. Layout analysis by increasing Stretch Factor for improving distance error.

Fig. 8. Simulation of Time Stretcher with proposed current mirror architecture with stretch factor $k=4$.

VI. RESULTS

To verify the performance in terms of output current variations, simulations were performed. Fig. 5 and Fig. 6 illustrates the DC characteristics of the current mirrors. The average output impedances for the *nmos* and *pmos*-based current mirrors are significantly above the requirements as presented in section III for an output voltage range of 0.5-2.5 V. From Monte Carlo simulations, the observed mismatch with 150 runs for *nmos* and *pmos*-based current mirrors are in the range of $-0.85\% \sim 1.01\%$ and $-0.78\% \sim 1.45\%$, respectively, for an 1.5 V output voltage. Schematics and post layout simulations were performed to analyze the impact of the parasitics involved, as shown in Fig. 9, Fig. 10 and Fig. 11. The design was evaluated and compared using four different stretch factors. Fig. 9 implies a growing schematic versus layout offset in stretched time as the stretch factor increases. This offset is due to the parasitics involved in the layout design causing charge injection in switches, variations in

Fig. 9. Transfer characteristics of time stretchers

Fig. 10. Distance error from schematic simulations.

Fig. 11. Distance error from layout simulations.

comparator propagation delay and differences in the reference level of the comparator. As shown in Fig. 10 and Fig. 11 the linearities achieved for schematic and layout are comparable and essentially independent on stretch factor.

VII. CONCLUSION

This paper presents an approach for the design of a time stretcher. Design constraints have been discussed for achieving output linearity and current mirror matching. The design was implemented for a precise magnitude of the stretch factors. Considering the non-linearity, transfer characteristics of our

time stretcher and current mirror matching, attaining a distance error of a few centimeters for a distance range of 10-15 meters was possible. This concept of a precisely matched time stretcher with high linearity gain can be used in conjunction with any time-to-digital converter to achieve an increased resolution and minimum distance error.

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