Constant g_m , rail-to-rail input transconductance stage with output common mode current compensation

Kirill Kozmin, Jonny Johansson
EISLAB, Luleå University of Technology
SE-971 87 Luleå, Sweden
E-mail: kirill.kozmin@ltu.se

Abstract—This paper presents a compensation structure to reduce the output common mode current of a rail-to-rail constant g_m transconductance stage. The transconductance stage is a differential structure with the input transistors biased in weak inversion. This results in low power consumption and a simple relation between g_m and tail currents. The constant g_m is achieved by doubling the tail current in the active differential couple when the other one goes to cut off. Together with constant bias current in the output stage this can result in common mode bias current flowing from the output depending on the common mode input voltage. The proposed solution eliminates this problem by variation of the bias current in the output stage in relation to the tail currents in the differential couples. The transconductance stage was manufactured in a $0.35\ \mu\text{m}$ CMOS process. Measurement results are presented together with simulation data. The compensation structure cancels the common mode output currents for common mode input signals up to a frequency of 7 MHz.

I. INTRODUCTION

In many applications such as operational amplifiers, comparators, analog buffers etc. a rail-to-rail input stage is needed [1], [2]. A common way to implement such a stage is to use parallel connected N and P differential couples together with a folded cascode output. To minimize power consumption CMOS transistors can be biased in the weak inversion region. In this case the transconductance of the parallel stage is proportional to the sum of the tail currents in the N and P couples. To keep the transconductance constant independently of the common mode input a circuit based on Wilson current mirrors can be utilized [3].

Usually a voltage output is used from a rail-to-rail stage. In the case of differential output a common mode feedback is then required to stabilize the output bias point. This generally decreases the bandwidth of the stage. However, if a current output is used, the following current amplifier takes care of the bias point and no common mode feedback is needed.

The use of a rail-to-rail constant g_m stage based on Wilson current mirrors can result in a common mode current at the output when the common mode input changes between rails. This common mode current can force the following current amplifier into saturation, which impairs its gain and bandwidth.

This paper presents a solution to the described problem. It is based on the idea of variation of the bias current in

the output stage in relation to the tail currents in the input differential couples. The following section describes the circuit structure and its functionality. Measurement and simulation results are presented in section three, followed by discussion and conclusions in section four and five.

II. CIRCUIT DESCRIPTION

The schematic of the input stage can be seen in figure 1. It is based on the well known structure of two parallel coupled P and N differential couples with a folded cascode current output stage [4]. The compensation circuit is marked with dashed line. The description of the circuit is given below. First we describe how the transconductance stage behaves without compensation circuit and based on this description show how the compensation circuit works.

The input transistors in the differential couples work in weak inversion, thus the transconductance of these transistors is proportional to the bias current. For the constant transconductance sum of tail currents in each couple should be constant. This is achieved with transistors MP3–MP10 and MN3–MN5 forming three Wilson current mirrors [5]. This circuit doubles the tail current in the active differential couple when the other couple goes to cutoff. When both differential couples are active they are biased with current I . Half of this current from each couple goes to respective input of the folded cascode, thus the output transistors MP15–MP16 and MN11–MN12 are biased with the current $\frac{3}{2}I$. When one input couple goes to cutoff the tail current in the active couple is doubled, i.e. it is $2I$. As the bias current in the output stage is constant at $2I$ the balance is broken: the current through one output transistor couple is $2I$ while through the other it is only I . This results in an output common mode current I .

The proposed solution to this problem is shown in figure 1 with dashed line and consists of transistors MP11–MP14 and MN7–MN10. This circuit forms variable current sources in the output stage proportional to the tail currents of the differential couples. Transistors MP11–MP14 and MN7–MN10 mirror half of the tail current to the opposite side of the output stage, i.e. the mirrors MP4:MP11 and MN4:MN8 are 2:1. When both differential couples are active they are still biased with current I . The bias current through the output transistors is now $2I$ because of the additional current equal to $\frac{1}{2}I$ mirrored from

Fig. 1. Schematic of the transconductance stage with compensation circuit within dashed line

the tail current source to the output. When one of the inputs is in cutoff the current through the other is doubled and half of it is mirrored to the opposite side of the output stage. This results in the same $2I$ current through the output transistors. Thus, no common mode output current flows at any input common mode voltage.

III. MEASUREMENTS AND SIMULATION

The transconductance stage was implemented in a $0.35 \mu\text{m}$ CMOS technology. Supply voltage is 3.3 V and bias current $2I = 15 \mu\text{A}$. To measure characteristics of the transconductance stage the output signal from it should be amplified. For this purpose a transresistance amplifier was used with transresistance of $10^5 \frac{\text{V}}{\text{A}}$ and bandwidth of 10 MHz . It was made of low offset, low input bias current general purpose operational amplifier AD8066 from Analog Devices as a transconductance input and two voltage gain stages around LMH6626 from National Semiconductor. The differential output signals from the transconductor were separately amplified.

The results presented in this section focus on the behavior of the compensation circuit. To investigate this two measurements were made.

- Measurement of output common mode current $i_{OUT,CM}$ as a function of the input common mode voltage $v_{IN,CM}$. This measurement is intended to show the low frequency, large signal efficiency of the compensation.
- Measurement of the frequency dependence of the common mode transconductance defined as

$$g_{m,cm} = \left. \frac{\partial i_{OUT,CM}}{\partial v_{IN,CM}} \right|_{V_{IN,CM}}, \quad (1)$$

where $V_{IN,CM}$ is a chosen bias common mode input voltage. This measurement is performed to evaluate the frequency span of the compensation functionality.

The measured results are in the following shown together with post layout simulation results.

Fig. 2. Common mode output current vs. common mode input voltage: simulation and measurements

Figure 2 shows measurement and simulation results of the common mode DC output current from the transconductance stage as a function of the common mode input voltage. The measurement was made with sinusoidal input signal at a frequency of 1 Hz . The compensation circuit effectively cancels the output common mode currents over the range of input common mode voltages.

In figures 3 and 4 the common mode transconductance $g_{m,cm}$ can be seen for common mode input voltages of 1.25 V and 1.85 V . These points were chosen because the transconductance is maximal there. This can be observed in figure 2 as the maximum slopes of the curve are located in these points. The compensation circuit bandwidth is estimated from figures 3 and 4 to about 7 MHz .

Table I summarizes the measured properties of the transcon-

Fig. 3. Common mode g_m vs. frequency for compensated and uncompensated g_m stage: $V_{cm} = 1.25$ V

Fig. 4. Common mode g_m vs. frequency for compensated and uncompensated g_m stage: $V_{cm} = 1.85$ V

ductor. Figure 5 shows a chip photo with main parts indicated.

IV. DISCUSSION

The transconductance stage shows good agreement between measurement results and simulation for low frequency. However a differential output signal was observed from the compensated transconductance stage when a common mode signal was supplied to the input. A possible reason for this is mismatch in the current mirrors in the compensation circuit. This results in a reduced common mode rejection ration (CMRR) when the compensation is used.

In the frequency dependent measurements for common mode input voltage of 1.25 V the agreement between simulations and measurements is good for low frequencies. The bandwidths from the measurements are somewhat lower than

Fig. 5. Chip photo

TABLE I

SUMMARY OF TRANSCONDUCTOR PARAMETERS

Parameter	Value
Supply voltage	3.3 V
Current consumption	104 μ A
Transconductance	120 μ S
Amplifier bandwidth (simulated)	170 MHz
Compensation bandwidth	7 MHz
Chip area	104x102 μ m ²

from the simulations. This can be explained partly by the higher capacitive load seen by the output in reality. Another reason is the bandwidth limitation of the transresistance post-amplifier, which makes the measurement more difficult in the high frequency range.

For the input common mode voltage of 1.85 V a quite high disagreement between simulation and measurements for the uncompensated transconductance stage can be seen. This is the result of decreasing transconductance in this point (see figure 2); the derivative of the simulated transconductance stage is higher than of the measured one.

V. CONCLUSIONS

This article has presented a common mode compensation circuit for a constant g_m rail-to-rail transconductance amplifier. The circuit cancels common mode output currents related to common mode input voltages by varying the bias current in the output stage in relation to the tail currents in the input differential couples. The measurement results show good agreement with simulated data and compensation bandwidth is estimated to be 7 MHz. However the circuit is shown to be sensitive to mismatch, which can result in differential output signals in response to a common mode input signal. The transconductance stage is manufactured in 0.35 μ m CMOS process. The transistors are biased in weak inversion, resulting in a current consumption of 104 μ A at a supply voltage of 3.3 V. The total design area is 104x102 μ m².

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