High Performance Sampled Current Measurement

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This paper describes the development of a current measurement method implemented on a controller card for use in electric motor drives for hybrid vehicles. The emphasis of the work is on the simulation and implementation of the current measurement system that is successfully evaluated. The current measurement saves power by saturating the transformer core between samples. Hence the name maximized saturation method (MSM).
This thesis work has been a great experience for me and the result would not have been reached without the help from many. I would first of all like to thank my supervisors Lars Lindberg and Erik Norberg at Kollmorgen and Prof. Kalevi Hyyppä at Luleå University of Technology for their support throughout the work. I would also like to thank Ulf Karlsson for his work as unofficial supervisor at Kollmorgen and the following staff that has helped me in various ways: Anders Permats for development and adaptation of software, Erik Rygran and Anders Lindberg for help with drive parameter set-up, Rickard Andersson for designing the layout of the PCB, Roland Lundström for teaching me the schematic tool, Ingemar Gréus for ordering the PCB and mounting components, Thord Nilson for helpful explanations of theory and design review, Håkan Röcklinger for making measurement equipment accessible and finally Kenneth Lindgren for his design reviews and measurement tips.

Max Wisten
5.1.2 Leakage Inductance ........................................... 26
5.1.3 Saturation Time .............................................. 27
5.1.4 Magnetizing Current ............................................ 28
5.2 DC Measurement .................................................. 32
  5.2.1 Supply Voltage Variations .................................... 32
  5.2.2 AD-converter input ........................................... 33
  5.2.3 Reference measurements DC ................................. 36
5.3 AC Test with Reactive Load ....................................... 40
  5.3.1 Power consumption .......................................... 42
  5.3.2 Temperature monitoring ..................................... 43

Chapter 6 – Evaluation .............................................. 51
  6.1 Current Measurement ........................................... 51
  6.2 Controller Card .................................................. 51
  6.3 Future Development ............................................. 52
Kollmorgen is a worldwide automation and controls company with extensive knowledge in motion technology. Their global design and manufacturing facility in Stockholm is currently developing electric motor drives for heavy hybrid vehicles. The drive units are intended for use with three-phase permanent magnet or induction motors and the first generation of the hybrid drive system is already in use.

The drive unit manages large currents through the phase windings of the motor, commonly denoted U, V and W. These currents need to be known for the unit to regulate the speed and torque of the motor. Measurements are done on two of the three phases of the motor. Since the voltages are high, galvanic insulation between control board and motor cables is a requirement. In the first generation drive, free-standing current transformer modules are used to measure the phase currents. These modules output an analog signal representing the corresponding phase current. Their construction is such, that the power consumption of the module increases with the phase current.

A patented method for measuring high currents in motor drive units has been developed and tested by Kollmorgen prior to this thesis work. The tests revealed promising results measuring 50Hz alternating current as high as 1400A RMS with less than 1% measurement error and a power consumption of 3.5W at a sampling rate of 4kHz[1].

## 1.1 Purpose

Kollmorgen’s hybrid controller, that in time of this writing, is used in test and production vehicles, is an important step for the company towards the very promising civil hybrid vehicle market. The drive unit consists of several sub-units. The unit managing all measurements, control and supervision is called the controller card. It is a physically separated PCB mounted in the casing of the drive.

The purpose of this thesis is to develop and fabricate a control card prototype for the second generation of hybrid drives. Particularly to further refine and evaluate the MSM
(Maximized Saturation Method) current measurement and introduce a new processor previously used by Kollmorgen in low voltage drives. Furthermore over-all simplification especially concerning the power supply of the controller card has been requested. The design goal of the current measurement is to measure peak currents of 1000A with a sampling frequency of 4kHz using the maximized saturation method in a realistic set up with motor and drive unit.
In any electric motor drive, keeping track of the current running through the motor windings is essential. In the case of the three-phase motor, two of the three phase currents are usually measured. Those two currents provide a base for calculating the third phase current. The method of measuring only two of the three phase currents is preferred due to reduced costs and complexity.

### 2.1 Shunt resistor

The most basic and intuitive method of current measurement is to run the current through a high precision electrically resistive component over which the voltage is measured. The method is simple and cheap, which makes it useful for low current applications where a non-galvanically insulated measurement is accepted. However, large current applications demands small valued resistors to keep the power dissipation to a minimum. This results in poor accuracy and significant sensitivity to noise. The method is often dismissed due to demands for galvanic isolation.

### 2.2 Current Transformer

The current transformer is a widely spread and simple to use device for measuring alternating currents. The device consists of a ferromagnetic core with a primary and a secondary winding. The secondary current is in the ideal case proportional to the primary current depending on the number of turns in the windings according to

\[ I_{\text{sec}} = I_{\text{prim}} \cdot \frac{n_{\text{prim}}}{n_{\text{sec}}} \]  \hspace{1cm} (2.1)
The main drawback of the current transformer is that in order to prevent saturation of the core, the size of the transformer must be increased with increasing current amplitude and decreasing frequency. With a larger core comes also increased weight and cost. Constant current (Direct Current, DC) can not be measured.

The total flux inside the transformer core with cross sectional area $A$

$$\Phi = BA$$

induces a current in the secondary winding when changing over time according to Faraday's law

$$e = n \frac{d\Phi}{dt} = nA \frac{dB}{dt}$$

Integration of both sides results in

$$\int e \ dt = nA \Delta B$$

If $e$ is a constant voltage $U_{\text{supply}}$, rearrangement gives

$$\Delta t = \frac{nA \Delta B}{U_{\text{supply}}}$$

which is an important relation for applications using active control of the transformer core flux. This topic is further discussed in chapter 3.

### 2.2.1 Hall-effect method

The current in the primary winding of a current transformer can be estimated by measuring the magnetic flux in the transformer core directly using a Hall-effect sensor. The sensor consists of a small metal plate over which a voltage is induced when the plate is exposed to a magnetic flux. Instead of using a secondary winding, a slot where the sensor is placed, is made in the transformer core. The resulting air-gap in the core makes it harder to saturate the transformer due to the low permeability of air $\mu_0$. An increased air-gap allows larger currents to be measured, but it also introduces problems since the core is no longer closed and the layout of the motor cable (primary winding) will affect the measured flux.

To avoid an impractically large air-gap in the core, a secondary winding can be used to cancel-out the field induced by the primary current. The flux is kept around zero using the Hall-effect sensor in a feedback loop to the controlling electronics. The measured current is proportional to the current in the secondary winding, as in the case of a standard current transformer.

Drawbacks of using a Hall-effect sensor are the price, accuracy and in case of the closed-loop method, high power consumption when measuring large currents.
A great thing would be to combine the high accuracy and low power consumption of the standard current transformer with the small transformer core and lack of saturation problems of the Hall-effect feedback method. Using a tiny core with a steep B-H-curve and an H-bridge controlled secondary winding taking the core out of saturation only during the time needed for a single measurement is what the MSM does to combine high accuracy with low power consumption.

### 3.1 Principle of operation

The main concept of the measurement method is to let the core be saturated as much of the time as possible and take it out of saturation only during the time required to make a measurement. When the core is saturated, current transformation and the resulting resistive loss is prevented. To desaturate the core a voltage must be applied to the secondary winding with a sign such that the resulting MMF (Magnetomotive Force) opposes that created by the primary current. The magnitude of the applied voltage is proportional to the rate of change of the core flux, meaning a higher voltage will desaturate (or saturate) the core quicker and also reduce the relative influence of the primary current on the desaturation time.

A voltage applied to the secondary winding in the wrong direction, i.e. pushing the core further into saturation, will result in a quickly rising secondary current. This kind of undesired saturation is detected by hardware when the secondary current reaches a certain level, which will end the pulse of applied voltage. When such a saturation is detected, the direction memory of the controlling logic will be changed meaning that the opposite current direction is assumed for the next measurement cycle. In order to make a valid measurement after the saturation detection the MSM always applies a second
voltage pulse with reversed direction after the desaturation pulse. The desaturation pulse is also called *forward* pulse and the reversed sign pulse is called *back*. The effect of the *forward* and *back* pulses are illustrated in figure 3.1a and 3.1b. The actual measurement is performed during the measurement state after the *back* pulse. During the measurement state the secondary core is shorted through a shunt resistor over which the voltage is measured. The measured voltage corresponds to the primary current and the maximum measurable current is ultimately limited by the reference used to detect saturation.

![Diagram](image)

**Figure 3.1:** Principle of operation in the BH-plane.

In figures 3.1a and 3.1b the *forward* pulse operates between point A and B, the *back* pulse between B and C and the drift caused by the primary current during the measurement state is the flux difference between point C and D.

### 3.2 Core material

The idea of deliberately saturating the core at all times but around measurements vastly changes the idea of a *good* transformer core. A classic current transformer would preferably be as hard to saturate as possible. This is implemented by a large cross sectional area and a choice of material with a high remanent flux density, $B_r$, meaning that a relatively linear relationship between the magnetic field intensity $H$ and flux density $B$, is maintained at high levels of field intensity. Figure 3.2 illustrates the meaning of the parameters $B_r$ (remanent flux density), $B_s$ (saturation flux density) and $H_c$ (coercive force).

In the case of the maximized saturation method, the core should be easy to bring into,
and out of saturation since this process will be repeated upon every measurement sample.

Transformer cores based on nano-crystalline or amorphous materials are supplied as tape-wound cores. This helps to limit induced rotating currents, also known as eddy currents in the core material, since the layers of the core are to some extent electrically isolated from each other [2].

3.3 Accuracy

The measurement accuracy of the maximized saturation method is dependent on a number of error sources. The two main general sources of measurement errors are the core properties and the electronics (shunt resistors, operational amplifier circuit and analog to digital converter).

If the B-H relationship is assumed to be linear in the region of measurement (and the relative permeability $\mu_r$ is considered to by infinite), the core properties determining the minimum measurement error are the coercive force, layer thickness of the core and resistance in the core material and between layers of the core. The layer thickness and the resistive properties of the core determine the limitation of eddy currents. Some eddy current effects can also be expected in the secondary winding of the transformer.

The coercive force of the core material is a hysteresis related property that will bring
an offset to the measured current. This offset is, on the contrary to eddy currents, not related to the magnitude of the measured current. In other words, one key parameter to look for when choosing a core material for the maximized saturation method, is a low $H_c$ (coercive force).

Eddy currents in the core and/or the secondary winding will during the measurement state induce an error current. The error current will add to the current drift caused by the non-infinite $\mu_r$ commonly known as magnetizing current, in the secondary winding. This current increases with the rate of change of the core flux which is proportional to the voltage over the secondary winding. The voltage over the secondary winding is determined by the current through the shunt resistance and will consequently increase with the measured current. The magnetizing current can be decreased by lowering the value of the shunt resistor and/or lowering the resistance of the secondary winding by increasing the wire thickness. This decreases the voltage drop over the secondary winding and hence the induced error current. The magnitude of the error current caused by eddy currents is difficult to calculate but the sum of the error currents can be measured.

3.4 Configuration of Windings

It has been shown that a basic single secondary winding setup is sensitive to the layout of the primary winding consisting of the motor cable running through the toroidal transformer. A solution to this problem is to use at least four secondary windings connected in parallel [1]. The phenomena is caused by unsymmetrical saturation and desaturation of the core which prolongs the time needed to desaturate the core prior to a measurement and saturate it afterwards. The effect vastly decreases the performance of the measurement method in terms of power dissipation and measurable current. See [1] for measurement results and deeper discussion of the subject.

The number of turns in the secondary windings is a trade-off between different causes of power dissipation. An increasing number of turns leads to higher winding resistance, leakage inductance and desaturation time. On the other hand the increased number of turns decreases the current in the secondary winding according to equation 2.1.

3.4.1 Leakage inductance

When the transformer core is fully saturated, the permeability of the core $\mu$ approaches the permeability of vacuum $\mu_0$. The remaining inductance of the transformer is called leakage inductance. The magnitude of the leakage inductance depends on the physical layout of the winding and is proportional to the number of turns squared. It is difficult to calculate but can be derived from measurements using

$$V = L \frac{di}{dt}$$  \hspace{1cm} (3.1)
which for a short time interval, after rearrangement can be approximated to

\[ L = \frac{V \Delta t}{\Delta i} \]  

(3.2)

The leakage inductance of the configuration with several parallel secondary windings can be calculated as

\[ L_{\text{resulting}} = \frac{L_1 L_2}{L_1 + L_2} \]  

(3.3)

### 3.5 Power dissipation

The power dissipation of the measurement system is important to the performance of the system itself, and to the demands on the power supply in the drive. The contributions to the total power dissipation of the measurement system can be divided to that of the transformer and the dissipation of the electronics including shunt resistors. The heat dissipated by the electronics is concentrated to the H-bridge with shunt resistors. The transistors of the H-bridge are generally well capable of conducting heat to the PCB, but should nevertheless have an as low as possible on resistance to minimize losses. Also the shunts can beneficially be as low valued as possible. Low valued shunt resistors decreases not only the power dissipated in the shunts themselves according to

\[ P = RI^2 \]  

(3.4)

but it also decreases the voltage over the secondary winding during the measurement state. The lower voltage decreases eddy currents in the core and winding which enables a more accurate measurement result. However, a low valued shunt resistor results in a low voltage corresponding to a specific current, which introduces higher demands on noise rejection and accuracy of amplification of the measured voltage. Concerning the secondary winding, assuming copper to be the material of choice, two basic design parameters mainly determine the resistive loss, namely the number of turns and the cross sectional area of the wire. The number of turns, the circumference of each turn and the cross sectional area of the wire determines the resistance of the secondary winding. Furthermore the number of turns is reverse proportional to the current in the secondary winding according to equation 2.1. An additional contribution to the transformer power dissipation is hysteresis losses of the core. This addition to the power dissipation should however be small considering soft magnetic material is preferably used in this application.

#### 3.5.1 Leakage inductance discharge

The maximum current through the secondary winding occurs immediately prior to the ending of a voltage pulse when saturation detection occurs. The current pulse will store energy in the leakage inductance of the secondary winding according to

\[ W_{L,\text{leak}} = \frac{L_{\text{leak}} I_{\text{sat}}^2}{2} \]  

(3.5)
This energy will then either be dissipated in the resistance of the secondary winding, shunt resistors and lower MOSFETs, or charge the capacitor bank through the fly-back diodes depending on implementation. The latter solution reduces the produced heat in all components since some energy is stored in the capacitor bank. In both implementations however, the leakage inductance will lead to unwanted heat dissipation, and should for this reason be minimized.

### 3.6 Power Supply

The voltage level supplied to the H-bridge connected to the secondary winding is a key design parameter since it determines the desaturation time and thereby, among other things, the maximum sampling frequency. The time needed to bring the core out of saturation and into the linear region can be calculated using equation 2.5 repeated below where $B_{ss}$ is the maximum flux density swing of the core material.

$$\Delta t = \frac{nA\Delta B}{V_{\text{supply}}}, \quad \Delta B \leq B_{ss}$$

If the desaturation pulse is too long, the change of flux exceeds $B_{ss}$ and the core will saturate in the opposite direction.

The current flowing through the secondary winding during the desaturation pulse will as soon as the core enters the linear region be

$$I_{\text{sec}} = \frac{I_{\text{prim}}n_{\text{prim}}}{n_{\text{sec}}} + I_{\text{error}}(V) \quad (3.6)$$

For large primary currents, assuming a single primary winding, this could be simplified and approximated to

$$I_{\text{sec}} = \frac{I_{\text{prim}}}{n_{\text{sec}}} \quad (3.7)$$

The supply voltage dip during the desaturation pulse must be within acceptable values to maintain a reliable operation without need for variable length timing pulses. Since the desaturation pulse is short, it is reasonable to assume all energy to be delivered by a capacitor bank. If the voltage dip is small, the energy delivered by the capacitor bank can be approximated to

$$W = VI_{\text{sec}}\Delta t \quad (3.8)$$

The energy stored in a capacitor is

$$W_{\text{cap}} = \frac{CV^2}{2} \quad (3.9)$$

Combining equation 3.8 and equation 3.9 and choosing the supply voltage $V$ as working point, the voltage change can be approximated to.

$$|\Delta V| = \left| V - \sqrt{V^2 - \frac{2VI_{\text{sec}}\Delta t}{C}} \right| \quad (3.10)$$
During the desaturation (normally forward) pulse, this change of voltage will be negative i.e. the capacitor bank is discharged. On the contrary, during the back pulse, the capacitor voltage will increase as the induced current will be of opposite sign in relation to the applied voltage. Note that equation 3.10 does not handle the sign of the voltage change.

The phenomena of power transfer between the primary winding and the capacitor bank in the power supply could overcharge the capacitor bank. For this to happen, the power must be switched off on the controller card so that no power is consumed while the motor must still be rotating, regeneratively producing a current through the transformer. To prevent such overcharge, some over-voltage protection/discharge mechanism should be installed in parallel with the capacitor bank.

### 3.7 Power Electronics: H-bridge

The need to apply a voltage over the secondary winding with alternating polarity is solved by the use of a so-called H-bridge. The H-bridge consists of four switching elements and is named after the shape of the circuit diagram illustrated in figure 3.3a to 3.3d.

![Figure 3.3: The states of the H-bridge used by the maximized saturation method.](image)

The switches shown in figure 3.3 are in practice implemented by MOSFETs of either the N-channel type or a combination of N- and P-channel transistors. The benefit of using a combination of P- and N-channel transistors is simplified drive circuitry. N-channel devices are cheaper and have lower on resistance than comparable P-channel devices which makes them popular even for high side switches in H-bridge designs. The problem when using an N-channel device as a high side switch is the need for a voltage higher than the supply voltage to enable maximum conduction through the transistor. This is in periodically switched applications usually solved by a so-called boot-strap capacitor.
and a drive circuit. The boot-strap capacitor is connected to the source terminal of the high side switch which is connected to the drain of the low side switch according to figure 3.3. Before the high side switch can operate, the boot-strap capacitor must be charged by operation of the corresponding low-side switch. When the low side switch conducts, the capacitor is charged through a rectifying diode from the drive circuit supply. The general boot-strap and drive circuit is illustrated in figure 3.4 where the two inputs are the controlling signal of the complementary output (IN) and the shut down pin (SD) that disables both outputs.

![Figure 3.4: Principal connection of an integrated hi/low side driver circuit.](image)

The minimum size of the boot-strap capacitance can be calculated as

\[
C_{\text{boot-strap}} \geq \frac{2Q_g + \frac{I_{gbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(\text{leak})}}{f}}{V_{cc} - V_f - V_{LS} - V_{min}}  
\]

(3.11)

where \(Q_g\) is the total gate charge, \(Q_{ls}\) is the level shift charge required per cycle, \(I_{Cbs(\text{leak})}\) is the leakage current of the boot-strap capacitor, \(f\) is the switching frequency, \(V_{cc}\) is the logic section supply voltage, \(V_f\) is the forward voltage drop of the boot-strap diode, \(V_{LS}\) is the voltage drop of lower MOSFET and load, \(V_{min}\) is the minimum boot-strap capacitor voltage. The leakage current of the boot-strap capacitor can be neglected in the case of a ceramic device [3]. MOSFETs contains a built in fly-back diode that often eliminate the need for an external diode in H-bridge applications. To prevent shoot-through, i.e. current running through both the upper and lower transistor in one branch of the H-bridge, a small dead-time is normally used in transitions between different states. A dead time is often implemented in hi/low side integrated gate driver circuits. If not, dead time can be achieved by a circuit such as illustrated in figure 3.5.
3.8 Controlling logic

The general description of the maximum saturation method in section 3.1 is not specific regarding certain details of operation. One such detail is the state of the H-bridge before the back pulse if the forward pulse is interrupted by a saturation detection. The options are to either open the H-bridge and hence let the secondary current flow through the fly-back diodes or to enter the measurement state and thereby let the secondary current flow through the lower transistors and the shunt resistors. The former solution has the benefit of a quick discharge of the energy that is stored in the leakage inductance during the saturation current pulse. The quick discharge reduces the power dissipation in the secondary winding, but the effect becomes negligible as the measured current increases. CHOOSING THE MEASURE STATE AS INTER-STATE BETWEEN THE FORWARD AND BACK PULSES RESULTS IN THREE ACTIVE STATES OF THE H-BRIDGE PLUS THE INACTIVE STATE OPEN BETWEEN THE MEASUREMENTS AS DESCRIBED BY FIGURE 3.3.

The timing is critical regarding all states of operation in the maximum saturation method. Furthermore the timing is dependent of implementation details such as supply voltage, transformer core dimensions and material, and turns ratio of the transformer. This suggests that the timing should be handled by a high resolution adjustable timer.
such as that found in a modern MCU. However, the MCU of choice might not have the capability and/or needed free resources to quickly respond to a saturation detection. A sensible control logic set up would be to let the MCU control the timing of the measurement allowing it to initiate the measurement sequence at the appropriate time with respect to the planned ADC sample. The saturation detection, current direction management and interruption of desaturation pulses upon saturation detection would be controlled by external hardware. The external hardware could be implemented with comparator/s and discrete logic circuits or a programmable integrated circuit such as a CPLD or even a simple external micro controller. The MSM measurement could also be implemented as a stand-alone module with sample and hold circuit and internal compensation for varying supply voltage. Such a module would if exact timing of samples is critical be controlled by a single timing pulse or possibly one timing pulse per channel of measured current. If timing is less critical as might be the case for high inductance loads and low sampling frequencies, the module could simply sample and hold at a sufficiently higher frequency than the application sample frequency.

### 3.9 Drawbacks and benefits

Drawbacks of the measurement method are the complexity of drive circuit and controlling logic, high timing demands and limited sampling frequency. Furthermore the power consumption increases with sampling frequency and will be higher for a system dimensioned for high peak currents, even when measuring a modest primary current.

Benefits are low power consumption, high accuracy, low cost, small transformer size and high current capability. The method is noise insensitive due to the low impedance of the shunt resistor circuit.
Although the new current measurement principle has been successfully tested\cite{ref1}, it had never been implemented for use in a variable frequency drive prior to this thesis work. Implementation in a drive for heavy hybrid electric vehicles is challenging since the characteristics of the measured current varies with respect to frequency, amplitude and wave shape during runtime.

A simulation model describing the non-linear current transformer and the secondary side control-logic including H-bridge has been developed in \textit{LTspice} \footnote{Design simulation software from Linear Technology, available free of charge on http://www.linear.com}. The model has been used to develop and evaluate a measurement algorithm capable of measuring alternating as well as direct current.

The hardware implementation includes two measurement channels referred to as channel V and W.

### 4.1 Non-linear Transformer

The transformer used in this work was simulated in \textit{LTspice} prior to implementation. The simulation model was then adjusted with respect to leakage inductance after measurements on the real transformer. The simulation model is a good approximation of the implementation, although the bipolar flux density swing of the real transformer was found to be slightly smaller than specified by the manufacturer.

#### 4.1.1 Simulation

The circuit simulator \textit{LTspice} provides two different models intended for simulation of non-linear inductances. One is a behavioural inductance specified with a mathematical expression for the flux. The other, which has been used in this work, is a hysteretic core.
model that defines the hysteresis loop with three material specific parameters; Coercive force \((H_c)\), remnant flux density \((B_r)\) and saturation flux density \((B_s)\). The hysteretic core model was chosen prior to the behavioural model because it is easy to use with material parameters provided by the core manufacturer. The upper and lower branches of the hysteresis loop are calculated as\(^4\)

\[
B_{\text{upper}}(H) = B_s \cdot \frac{H + H_c}{|H + H_c| + H_c(B_s/B_r - 1)} + \mu_0 H 
\]

\[
B_{\text{lower}}(H) = B_s \cdot \frac{H - H_c}{|H - H_c| + H_c(B_s/B_r - 1)} + \mu_0 H 
\]

The resulting hysteresis loop for \(H_c = 0.3\)A/m, \(B_r = 0.55\)T and \(B_s = 0.58\)T can be seen in figure 4.1. Note that \(H_c\) determines the point of intersection on the field strength axis, while the vertical magnetic flux density axis is intersected at \(B = B_r\).

Besides the magnetic properties of the core material the model requires a few parameters describing the physical dimensions of the transformer core, namely the magnetic length, the cross sectional area of the core and the number of turns in the winding. Yet another parameter exists to describe an air gap in the core, but it is not needed in this work. Since the model does not take into account the shape of the core and the
distribution of the winding, some leakage inductance must be added in the circuit in series with the non-linear inductance if the leakage inductance is of significance to the application. Also a series resistance can be specified internally in the inductor model or placed externally in the circuit. Leakage inductance is in general difficult to calculate and its magnitude has in this case been established by measurements and then been fed back to adjust the simulation model. The actual current transformation is modelled as a coupling factor between two inductances. Since the non-linear inductance model does not allow such a coupling factor, a significantly larger inductance is connected in parallel with the non-linear secondary inductance. This large parallel inductance is then coupled to the primary inductance. According to equation 3.3 this connection is valid since the non-linear inductance will be the smaller inductance by far in all modes of operation.

4.1.2 Implementation

The core used is made of the material Vitrovac 6025Z, developed for use in magnetic amplifier chokes by VAC\(^2\). The material has an extremely steep and narrow hysteresis curve, meaning quick saturation and low hysteresis measurement error. Table 4.1 summarizes the properties of the transformer. The material data originates from [5] and is given for 25 \(^\circ\)C if not specified otherwise. The value of \(\mu_r\) is estimated from a graph.

The specific model of the core was chosen for its small cross sectional area and large inner diameter enabling a thick primary conductor. The number of turns in the secondary winding and hence the turns ratio of the transformer was chosen to result in good trade-off between a low maximum secondary current and a quick desaturation with the chosen desaturation voltage. The winding consists of four parallel coupled sections each consisting of 200 turns of wire. This results in a secondary current of 5A while measuring 1000A primary current. The secondary current will flow only for a period in the order of 20\(\mu\)s each sample, which allows relatively thin wire in the secondary winding. Each section of the winding was wound as twenty turns of ten parallel threads to speed up the work. The wires were then connected in series to result in the equivalent of 200 turns. A wire thickness of 0.25mm was experimentally proved to be appropriate to fit in one layer.

4.2 Controlling logic

The H-bridge controlling the secondary winding must be able to realize four different states to implement the MSM. The states are forward, back, measure and open. In order to minimize the demands on the MCU in terms of available connections and hardware timers, some signal generation and control of the H-bridge was decided to be handled by external hardware. The signals generated by the MCU are blue in figure 4.3.

\(^2\)Vacuumschmelze GmbH & Co.
Table 4.1: Transformer data

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core material</td>
<td>Vitrovac 6025 Z</td>
</tr>
<tr>
<td>Saturation flux density, $B_s$</td>
<td>$0.58T$</td>
</tr>
<tr>
<td>Bipolar flux density swing, $B_{ss25^\circ C}$</td>
<td>$1.15T$</td>
</tr>
<tr>
<td>Bipolar flux density swing, $B_{ss90^\circ C}$</td>
<td>$1.0T$</td>
</tr>
<tr>
<td>Squareness, $B_r/B_s$</td>
<td>$&gt; 0.96$</td>
</tr>
<tr>
<td>Curie Temperature, $T_C$</td>
<td>$240^\circ C$</td>
</tr>
<tr>
<td>Static coercivity, $H_c$</td>
<td>$0.3 Am^{-1}$</td>
</tr>
<tr>
<td>Relative permeability, $\mu_r$</td>
<td>$4 \cdot 10^4$</td>
</tr>
<tr>
<td>Core shape</td>
<td>Toroidal</td>
</tr>
<tr>
<td>Inner diameter</td>
<td>$35mm$</td>
</tr>
<tr>
<td>Outer diameter</td>
<td>$37mm$</td>
</tr>
<tr>
<td>Height</td>
<td>$2.5mm$</td>
</tr>
<tr>
<td>Winding type</td>
<td>Four parallel 200 turns</td>
</tr>
<tr>
<td>Winding wire diameter</td>
<td>$0.25mm$</td>
</tr>
<tr>
<td>$20^\circ C$ resistance, $R_{C_{u20^\circ C}}$</td>
<td>$0.25\Omega$</td>
</tr>
<tr>
<td>$100^\circ C$ resistance, $R_{C_{u100^\circ C}}$</td>
<td>$0.3\Omega$</td>
</tr>
</tbody>
</table>

Figure 4.2: The current transformer with four parallel windings in different stages of construction.

The simulated control logic is designed to be easily translatable to hardware. NAND gates are frequently used as they are cheap versatile building blocks available with Schmitt-trigger inputs. The NAND gate is in several logic families the simplest form of gate[6]. For these reasons most of the control logic is constructed by NAND-gates.
4.3 Saturation detection

Figure 4.3: Blue signals are generated by the MCU. The forward signal is generated by external hardware.

Figure 4.4: Logic consisting of NOR-gates creates the forward pulse out of the signals enable and back.

In the simulated circuit the logic gates are represented by idealized models provided with the simulation program. Although most of the external logic is implemented using NAND-gates, the circuit creating the forward pulse in figure 4.3 is built up of NOR-gates as this solution fits into one quad package. The forward pulse logic is shown in figure 4.4.

4.3 Saturation detection

When the transformer core saturates the permeability drops towards $\mu_0$ and the current will increase fast, only limited by the leakage inductance and the supply voltage, neglecting resistive limitations. Saturation is detected by hardware as a voltage over one of the shunt resistors that is larger than the voltage corresponding to the maximum measurable primary current. The comparator LM2901 and a reference voltage is used to
detect saturation. A simulation model for the LM2901 provided by Texas Instruments\(^3\) was used.

### 4.4 Adaptation to changed current direction

The sign of the applied desaturation voltage during the forward pulse is to be such that the resulting magnetic field is opposite in direction with respect to that created by the primary transformer winding i.e. the motor cable. If the primary current changes direction, the applied voltage will drive the core even further into saturation and the forward pulse is cancelled by the saturation detection logic. The saturation signal (which is active low) is clocked into a D-latch controlling the direction memory at the falling edge of the enable pulse. The timing of the pulses is illustrated in figure 4.9. The circuitry used in the simulation which is constructed to be directly translatable to hardware is shown in figure 4.5.

![Figure 4.5: Logic handling changes in current direction. Interconnecting wires to the symmetrical counterpart of the circuit are those leaving at the bottom of the figure.](image)

#### 4.5 H-bridge

The H-bridge was simulated in two versions. The first using idealized switches representing NMOS transistors with drivers and the second using a configuration of combined P-

\(^3\)Texas Instruments, http://focus.ti.com/docs/prod/folders/print/lm2901.html
4.6. Simulated Measurement Cycle

and N-channel MOSFETs, with gate drivers consisting of logic level devices only. The latter solution is of interest since it is cost effective, but was not to be implemented in this thesis work due to its limitations regarding supply voltage imposed by the P-channel MOSFET. Specifically, a PMOS device will have a higher on resistance than the corresponding N-channel MOSFET. For this reason the availability of P-channel devices of competitive performance is limited above certain maximum drain-source voltages. The H-bridge and transformer circuit using ideal switches is shown in figure 4.6.

Figure 4.6: The simulated transformer circuit

4.6 Simulated Measurement Cycle

A visual summary of the simulation results consists of figures 4.8, 4.9 and 4.10. The simulated circuit is represented in figures 4.4, 4.5 and 4.6. The signals enable, comparator one input and comparator two input along with the saturation reference voltage level, direction and the primary current are present (from top and down) in figure 4.8. The same signals with addition of the back signal in the top-most plot pane are visualized in figure 4.9 which illustrates the timing of the direction signal toggle as a result of the saturation detection.

Figure 4.10 is a zoomed in transient simulation of the differential voltage over the shunt resistors along with the timing signals.
Figure 4.7: The simulated P- and N-MOS circuit.

Figure 4.8: Overview of signals.
4.6. Simulated Measurement Cycle

Figure 4.9: Timing of direction change.

Figure 4.10: Simulated differential voltage at 1000A primary current. (1mv/A)
The main purpose of the measurements was to verify the function of the implementation and reveal any unforeseen issues. The two main parts of the work done is a DC measurement with reference measurement and an implementation evaluation in a high voltage motor drive unit.

### 5.1 Transformer Testing and Verification

To verify the relevance of the simulation results four crucial main properties of the transformer were measured. Those properties are the electrical resistance, the leakage inductance, the saturation time-voltage area and the minimum error current of the transformer.

#### 5.1.1 Resistance

The resistance of the transformers secondary winding was measured with a simple setup consisting of a DC power supply and two multimeters, one measuring current and the other voltage drop over the winding.

The measurement was done at room temperature, leaving the winding resistance at any other temperature to be calculated as

$$R_T = R_{ref} + \alpha(T - T_{ref})R_{ref}$$

where $\alpha = 0.0039$ is the temperature coefficient of copper[7]. A summary of the measurement is given below:

<table>
<thead>
<tr>
<th>current</th>
<th>voltage</th>
<th>$R$</th>
<th>$R@100^\circ C$ (calculated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100mA</td>
<td>25mV</td>
<td>0.25$\Omega$</td>
<td>0.3$\Omega$</td>
</tr>
</tbody>
</table>

More transformer data and details concerning the secondary winding are collected in table 4.1.
5.1.2 Leakage Inductance

Inductance can be calculated from a simultaneous measurement of a voltage applied over the secondary coil and the rate of change of the resulting current according to equation 3.2. Figure 5.1 illustrates the current increase resulting from a voltage step over a single winding out of four parallel in the secondary winding of the transformer. The corresponding measurement result from the finished parallel coupled winding is shown in figure 5.2. Note that the increasing current is pretty much a straight line shortly after the voltage is applied, which makes it a good region for the inductance calculation. In the case of the single winding the leakage inductance is read from figure 5.1 as

\[
L_{\text{leak, single}} = \frac{V \Delta t}{\Delta i} = \frac{27 \cdot 2 \cdot 10^{-6}}{3} = 18 \mu H
\]  

(5.2)

The same procedure for the parallel case gives based on figure 5.2:

\[
L_{\text{leak}} = \frac{23 \cdot 2 \cdot 10^{-6}}{9.5} = 4.8 \mu H
\]  

(5.3)

which is roughly a quarter of the single winding leakage inductance, as expected.

Figure 5.1: Voltage over and current through one out of four secondary windings as a base for leakage inductance calculation.
5.1. Transformer Testing and Verification

Figure 5.2: Voltage over and current through four parallel secondary windings as a base for leakage inductance calculation.

5.1.3 Saturation Time

The time required to bring the core from saturation in one direction of magnetic flux to saturation in the opposite direction depends on the voltage over the secondary winding as described by equation 3.6. The circuit used for the measurement is schematically presented in figure 5.3.

Figure 5.4 indicates a saturation time of 14.4 µs at an applied voltage of 30V. According to equation 2.5 the saturation time can be written as

$$\Delta t = 14.4\mu s = \frac{nA\Delta B}{V}$$

Insertion of numerical values for the number of turns, cross-sectional area and the applied voltage with rearrangement of terms,

$$\Delta B = \frac{\Delta t V}{nA} = \frac{14.4 \cdot 10^{-6} \cdot 30}{200 \cdot 2.5 \cdot 10^{-6}} = 0.84T \tag{5.4}$$

which is in the order of, although lower than the bipolar flux density swing $B_{ss25\circ C} = 1.15T$ specified by the manufacturer.
5.1.4 Magnetizing Current

The magnetizing current was measured while a voltage was applied over the secondary winding causing a drift in flux density until the point when the core was saturated.
The purpose of the measurement was to estimate the influence of eddy currents in the transformer core and winding, adding to the unavoidable offset current caused by the coercive force of the material. Figures 5.6, 5.7 and 5.8 shows the applied voltage and resulting current for 0.5V, 5V and 25V respectively. The current is measured with a current probe\(^1\).

The estimated mean current at the plateau of all the measurements are plotted in figure 5.9. The shape of the current steps in the measurements are not shaped as ideally as one might expect. The current waveforms reveal an overshoot that could be a result of parasitic inductance and capacitance in the measurement circuit.

Figure 5.5: Magnetizing current at 0.1V. 2mA/div on channel two. Applied voltage on channel one.

\(^1\)Tektronix A6312 100MHz current probe with Tektronix AM503B current probe amplifier.
Figure 5.6: Magnetizing current at 0.5V. 2mA/div on channel two. Applied voltage on channel one.

Figure 5.7: Magnetizing current at 5V. 2mA/div on channel two. Applied voltage on channel one.
Figure 5.8: Magnetizing current at 25V. 2mA/div on channel two. Applied voltage on channel one.

Figure 5.9: Magnetizing current at different voltages. The first five voltage values are: 5mV, 10mV, 50mV, 100mV and 200mV.
5.2 DC Measurement

Evaluation of the accuracy of the implemented current measurement method was done on direct current discretely varied using a laboratory power supply and a high accuracy reference measurement\(^2\). The sampling was done simultaneously on both channels (V and W) with the same primary conductor running through both transformers as shown in figure 5.12a.

5.2.1 Supply Voltage Variations

The DC set-up with the same current running through both transformers constitutes the worst case scenario in terms of discharge of the H-bridge capacitor bank due to transformation of primary current. Figure 5.10 shows the variations of the 30V supply to the H-bridges when 1500A DC runs through both transformers with a measurement cycle time of 25\(\mu\)s, which is longer than the later implemented 20\(\mu\)s.

![Figure 5.10: Voltage variations in capacitor bank with 1500A DC simultaneously sampled with 4KHz on both channels. 5V/div on channel 3.](image)

\(^2\)LEM 150-S current measurement module with 1\(\Omega\) shunt resistor and Hewlett Packard 3456 Digital voltmeter.
5.2. DC Measurement

5.2.2 AD-converter input

The input at the analog to digital converter (ADC) is the voltage corresponding to a primary current that is available for sampling by the MCU. The timing of the sampling in relation to the control pulses (forward and back) to the MSM-logic is critical, since the short measurement state is the key to low power consumption of the method. For this reason good knowledge of the sampled signals shape is important.

In the figures 5.11a to 5.11p the 25µs long enable pulse is shown together with the back pulse and the input voltage to the analog to digital converter for different primary currents.

(a) 100A DC  (b) -100A DC

(c) 500A DC  (d) -500A DC
(e) 1000A DC
(f) -1000A DC

(g) 1100A DC
(h) -1100A DC

(i) 1200A DC
(j) -1200A DC
5.2. DC Measurement

(k) 1300 A DC

(l) -1300 A DC

(m) 1400 A DC

(n) -1400 A DC
Figure 5.11: The ADC-input on channel three and the enable and back pulse on channel one and two respectively. The offset is such that 1.5V on channel three represents 0A primary current. The gain is 0.97mV/A.

The characteristic shape of the waveform on channel three in figures 5.11a to 5.11p describes the operation of the H-bridge. During the forward pulse the secondary current flows through one of the two shunt resistors. The forward pulse is active between the rising edge of the enable and back pulse. Upon the transition between the forward state and back state a spike in the output voltage can be noticed for high primary currents as the secondary current moves from one shunt resistor to the other. If the secondary current flows down through one shunt resistor during the forward state, it will flow up through the other during the back state and thus the differential measurement output voltage will keep its sign of polarity. During the measure state the secondary current circulates through both shunt resistors which is noticed as a twice as high differential output voltage. For primary currents above 1300A the differential output voltage drops gradually during the measurement state as can be seen in figures 5.11k to 5.11p. This indicates that the transformer core no longer operates in the linear region of the BH-curve but instead drifts towards saturation caused by the primary current.

5.2.3 Reference measurements DC

The reference measurements were performed with a set-up consisting of a DC-supply and a current measurement module with shunt resistor connected to a precision voltmeter. The performance of the complete measurement system was considered, hence the output from the ADC was compared to the reference measurement. To render possible large primary currents the primary conductor was fed nine turns through the transformers as shown in figure 5.12a. One of the DC-supplies used as well as the digital voltmeter is illustrated in figure 5.12b.
5.2. DC Measurement

(a) Primary conductor nine turns in each transformer. 
(b) DC-supply and voltmeter (top).

Figure 5.12: The basic elements of the DC reference measurement.

The result of the first measurement of primary current in the interval -1550A to 1550A is illustrated in figures 5.13a and 5.13b. The ideal ADC value for each current calculated from the reference measurement output was compared with the actual ADC value and the result with the difference in ADC value on the Y-axis is plotted in figures 5.14a and 5.14b for channel V and W respectively.

Figure 5.13: DC sweep -1550A to 1550A. Gain: 0.75A/ADC-increment.
Figure 5.14: ADC error, -1550A to 1550A. Gain: 0.75A/ADC-increment.

A comparison between figures 5.14a and 5.14b reveals a difference in error of benefit to channel W. This was noticed during the measurement and a suspicion of influence of heating of the core arose. The measurement procedure was as follows: Adjust current limit on DC-supply, activate DC-supply output, read reference measurement, channel W ADC-value, channel V ADC-value and disable DC output. Since the high currents caused heating of the primary conductor and therefore also the transformer cores, the non-simultaneous reading of ADC values could result in different operating temperatures between cores at measurement. To test this, a new measurement on channel V only was performed when special care was taken to make a quick reading before excessive heating could occur. The result is represented by figures 5.15a and 5.15b.

To better evaluate the performance of the measurement system with respect to accuracy the gain of the differential measurement of the shunt voltages was increased. This reduced the maximum measurable peak current to approximately 800A.
5.2. DC Measurement

Figure 5.15: Measurement number two on channel V -1550A to 1550A.

Figure 5.16: DC sweep -800A to 800A. Gain: 0.39A/ADC-increment.
The large offset current revealed by figures 5.17a and 5.17b corresponds to a practically constant offset current of 8A over the measured range. The result was quite a surprise, and even though not causing a direct failure, finding the cause of the unexpectedly large offset became a priority for the next set of measurements. In the measurements above a primary winding consisting of nine turns of 8.37mm² (8AWG) copper wire was used. In an attempt to reduce the offset current a new measurement with a single turn primary winding was performed. The result is shown in figures 5.18a to 5.19b.

The results of the single primary measurement show an offset current of up to one ADC-increment corresponding to 0.39A. This offset with a distinct hysteretic behaviour seems to be a predictable offset error current. Furthermore figures 5.19a and 5.19b indicates a total offset affecting the positive as well as negative current range. The latter offset is likely to be at least partly caused by remanence effects.

5.3 AC Test with Reactive Load

To verify the capability of the implementation to function in a motor drive application, the controller card was installed in a high voltage drive in a laboratory set-up with a reactive load. The drive(partly covered by a plastic lid), control box and an oscilloscope plotting the rotating current vector is visible in figure 5.20.

The drive was connected to a PC by CAN-bus. Thereby the drive unit could easily be monitored and configured using an application called DriveTool developed by Kollmorgen. Figures 5.21a and 5.21b shows the display of two transient records of the current measurement ADC samples requested by and plotted in DriveTool.
Bus voltage to the drive unit was supplied by laboratory voltage supply units. The voltage used in the test was in the span 400V to 600V. The output was during the performance tests of the current measurement regulated by an open loop algorithm to avoid oscillations in the output, but closed loop current control was also successfully tested.
Figure 5.20: Drive setup with high voltage supply.

![Image of drive setup](image)

(a) 1.4ARMS, 60Hz  
(b) 150ARMS, 6.7Hz

Figure 5.21: Transient record of the drive measuring current on channel V and W. AD-converter bits on the y-axis versus sample number on the x-axis. Sample frequency is 4kHz.

### 5.3.1 Power consumption

The two main causes of power consumption of the current measurement implementation is the current rush associated with saturation detection and the transformed current that linearly depend on the primary current. Both the saturation detection loss at
small currents and the transforming losses (at higher currents) increases with sampling frequency. However only the saturation dissipation increases with the frequency of the primary current, as a saturation will occur at every zero crossing of the measured current. The increase will be linear with frequency, except for the case of low primary current amplitude (in the order of 1A or less), when saturation losses will primarily be a function of sampling frequency. The latter phenomena results in a noticeable increase in power consumption for primary currents below the threshold level i.e. when the primary current is not big enough to drive the core back into saturation between samples.

Figures 5.22 to 5.31 shows the current to the capacitor bank of the measurement circuit on channel one and the 20μs enable pulse on channel two. The current to the capacitor bank was measured with a current probe. The mean value of the current is shown as a MEASURE parameter in figures 5.22 to 5.31. The supply voltage is approximately 30V.

![Graph showing current consumption](image)

**Figure 5.22:** Current consumption on channel 1, 20mA/div. 0A primary current.

### 5.3.2 Temperature monitoring

An infra-red camera was used to determine the operating temperature of the measurement system. Figure 5.32b illustrates the temperature variations of the logic circuitry and H-bridges with shunt resistors. The components with the highest temperature are dual NFET SO-8 packages that can be seen next to the bundles of shunt resistors in figure...
Figure 5.23: Current consumption on channel 1, 20mA/div. 36ARMS, 7Hz primary current.

5.32a. Figure 5.33 shows a representation of an infra-red image of the motor cable running through one of the measurement transformers while a primary current of 250ARMS flows through the motor cable and measurement is performed. The figure illustrates that the motor cable is significantly warmer than the secondary winding, which indicates low power dissipation in the measurement transformer.
Figure 5.24: Current consumption on channel 1, 20mA/div. 48ARMS, 60Hz primary current.

Figure 5.25: Current consumption on channel 1, 20mA/div. 64ARMS, 60Hz primary current.
Figure 5.26: Current consumption on channel 1, 20mA/div. 80ARMS, 60Hz primary current.

Figure 5.27: Current consumption on channel 1, 20mA/div. 120ARMS, 60Hz primary current.
Figure 5.28: Current consumption on channel 1, 20mA/div. 152ARMS, 60Hz primary current.

Figure 5.29: Current consumption on channel 1, 20mA/div. 200ARMS, 60Hz primary current.
Figure 5.30: Current consumption on channel 1, 20mA/div. 273ARMS, 60Hz primary current.

Figure 5.31: Current consumption on channel 1, 20mA/div. 280ARMS, 60Hz primary current.
5.3. AC Test with Reactive Load

(a) Controller logic and H-bridges  (b) Representation of infra-red picture. The numbers to the left are max, mean and min temperature of the marked box.

Figure 5.32: The controlling logic circuits and H-bridge with shunt resistors and the corresponding representation of an infra-red picture while operating at 200ARMS, 50Hz. The hotspots are the dual NFET packages.

Figure 5.33: Motor cable running through measurement transformer. The bright line running diagonally through the figure is the significantly warmer motor cable. Current running is 250ARMS, 50Hz.
6.1 Current Measurement

Increasing measurement offset with increasing number of primary turns was discovered.

Drawbacks of the measurement system are complexity of drive circuit and controlling logic as well as limited sampling frequency. The power consumption increases with sampling frequency and will be higher for a system dimensioned for high peak currents, even when measuring a modest primary current.

Benefits of the current measurement system are low power consumption, high accuracy, low cost, small size, insensitive to noise, high current capability and great flexibility of implementation regarding system integration.

The highest power consumption can be expected at no (or very low valued) motor current.

The implementation is well capable of measuring 1000A peak current with an error below 1% at a sampling frequency of 4kHz in the configuration presented in this paper.

6.2 Controller Card

Although the focus of this paper is the simulation and implementation of the MSM current measurement, a complete controller card prototype was developed in the process. Only some of the many functions of the controller card were tested, but those that were tested seemed to work satisfactory. The tested features besides the current measurement part include power supply, PWM outputs (voltage level shifters), DC-bus voltage measurement and CAN-communication.
6.3 Future Development

Lower shunt resistances would improve accuracy at high currents and reduce power dissipation. Using a programmable logic device such as a CPLD or even a microcontroller would reduce board space usage of the controlling logic. Adaptable timing with respect to supply voltage and/or amplitude of the measured current could be implemented to reduce power consumption and increase accuracy. Saturation detection could be implemented as a differentiating circuit eliminating the need for a large current amplitude to detect saturation. The use of differentiating has the potential of reducing power consumption, particularly at low primary currents.

If the measurement method is to be implemented in an independent module, use of a microcontroller with dual integrated comparators could be beneficial.

Remanence effects should be investigated.
Bibliography


