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Abdelghani Renbi and Jerker Delsing
Luleå University of Technology
Luleå, 971 87 Sweden

Ph: +46920491093 ; Fax: +46920491399

Email: Abdelghani.Renbi@ltu.se, Jerker.Delsing@ltu.se

A novel production process for 10 μm microvias.

Abstract

This work investigates the capability of drilling and metallization of microvias of diameter less than 10 μm with aspect ratios of 1-10, using a fully additive process.

The microvia has been produced using a sequential build up layer of urethane through which the via has been produced. The urethane layer is applied using spin-coating. Current process setting produces a 15 μm layer thickness. For thicker urethane, multiple layers are applied. Drilling of the via-hole through is made using 266 nm UV laser.

The metallisation of the via-hole was made using a process called Covalent Bonded Metallisation (CBM). This process modifies the urethane surface by a grafting process where polymers are covalently bonded to the surface where metallisation is desired. A roughly 5 μm thin film of the used grafting solution is applied to the substrate surface. The grafting process is initiated by laser which draws the patterns where copper is desired.

After laser drawing, the substrate is cleaned with deionized water. Next, the substrate is through a commercial chemical-copper process which builds copper only at the laser initiated patterns. Copper thicknesses of 1 μm is easily achievable. To increase the copper thickness, the substrate may be run into thick building chemical-copper process to achieve thicknesses up to 8 μm .

Key words

Microvia, Electronics packaging, PCB interconnect, Laser drilling, Wire Bonding, SBU, HDI, Wafer Level Packaging

I. Introduction

Microvia technology is an essential part to build multilayer circuit boards for higher functionality/area and higher performance electronics. State of the art System in Package (SiP) wiring requires high density interconnects between stacked silicon dies in e.g. Through-silicon via (TSV) and Wafer Level Packaging (WLP) technologies [1].

As figure 1 illustrates, WLP has evolved to 2D Multi-chip module (MCM) with embedded passives and to 3D SiP with face to face (F2F) packaging, gaining higher level of integration.

These technologies uses Cu redistribution layer (RDL) and microvias to create conductive paths. This RDL is processed using seed layer and well known subtractive process. To fan-out I/O interconnections to the external soldering balls, interposers and molds are used [2]. The major challenges exist in the feature-size

of interconnects where width and proximity need to support small pitch i.e (< 40 μm).

Several technologies are used to form blind and buried microvia for interconnecting copper layers in circuit boards such as laser drilling, photolithography and plasma etching.

Due to high resolution capability and better flexibility, laser drilling remains as the most dominant and promising technology for small feature size microvia.

Several laser drilling processes have been developed to drill small via, which include, YAG, CO₂ and UV lasers, where the wavelength, energy density, substrate material and its thickness are the main factors that control the smallest via size.

Fig. 1 Trends of Wafer Level Packaging (WLP) based SiP.

II. Trends for microvia technology and related work.

There exist three different technologies for via formation.

The first technology use plasma to etch material for hole formation. The dielectric material is often resin coated copper (RCC). In addition to the expenses on special vacuum equipment, plasma etching is the least promising method to small feature size, where about 75 μm via hole diameter can be achieved on about 25 μm thick polyimide.

The second technology which has initiated the evolution of High Density Interconnect (HDI) boards is the photo-via. This technology uses photo-imaginable dielectric material and lithography patterning. On the other hand it is expensive due to the special dielectric material also its feature size which is limited to about 25 μm for both hole diameter and depth.

Laser drilling is the third and the most promising technology for smaller via hole formation. With laser technology, down to 5 μm can be achieved as via hole diameter in 5 μm thick material. This is controlled by the wavelength, energy density, substrate material and its thickness as the main factors.

Within the aforesaid technologies, the aspect ratio Depth:Diameter is an important factor which describes the ability of keeping smaller feature size with thicker material. This contribute to higher integration level by keeping the vias smaller and substrates ticker. Among those three technologies, UV laser drilling becomes the necessity for higher aspect ratio. Figure 2 sheds light on the ability of each technology.

Table. 1 Via hole aspect ratio using conventional technologies and mainstream UV lasers.

Aspect ratio= Thickness (μm):Diameter (μm)

UV lasers	PID	Plasma etching
Wavelength = 248 nm 10:10 = 1 on epoxy composite [3][4]	25:25 = 1 on epoxy composite [7]	25:75 = 0.33 On polyimide [8]
Wavelength = 266 nm 8:20 = 0.4 on epoxy composite [3]		
Wavelength = 308 nm 5:5 = 1 on polyimide [5]		
Wavelength = 355 nm 35:25 = 1.4 on polyimide [6]		

In general, there exist only couple of works which have reported the formation of ultra small microvia. In [3] and [4], the authors have affirmed the success of 10 μm microvias in 10 μm thick dry film dielectric with 248 nm KrF excimer laser on ZS100 polymer. On the other hand, this process is still semi-additive process (SAP) where Cu seed layer is initiated and etched afterward. Thus, the associated challenges with Cu seed based SAP process are still to be faced [9].

III. Semi-additive process challenges with small feature size.

Advanced fan-out WLP requires interconnects in the range of 1 μm wide. With the current material technology and semi-additive process (SAP), this feature-size is not feasible due to the following [9]:

- 1) Surface roughness for better Cu seed adhesion limits this range of feature size.
- 2) Etching process causes deteriorate the shape of the interconnects.
- 3) Trace delamination due to insufficient bonding.
- 4) With ultra small proximity, palladium residues tends to cause electrical shorts.
- 5) Non-uniform Cu thickens after the electroplating.

IV. Process Description

This section introduce a novel fully additive process using Covalent Bonded Metallisation (CBM).

The process permits to deposit copper on a selected area on non-metallic substrate using patterning with UV lithography or UV lamp and mask.

A layer of urethane or polyimide is spin-coated on the top of substrate. Our current process setting produces a

15 μm ayer thickness of urethane. For thicker urethane or polyimide, multiple layers are applied.

After laser drilling, a roughly 5 μm thin film of a grafting polymer solution is applied to the substrate surface. The grafting process is activated by UV laser which draws the patterns where copper is desired.

Using UV light the substrate surface is activate such that polymers are connected to the surface, building a nanoscale “forest” as illustrated by figure 2. This polymer forest allows perfect palladium and copper adhesion. Thus, no surface modification for roughness nor seeding copper layer. The modification of the surface is done by a grafting process where polymers are selectively covalently bonded. This is the main advantage of this process for supporting smaller feature size below 5 μm .

Fig. 2 Process description showing grafting polymer activation.

After laser drawing, the substrate is cleaned with deionized water. Next, the substrate is run through a commercial chemical-copper process which builds copper only at the laser initiated patterns. Copper thicknesses of 1 μm is easily achievable. To increase the copper thickness, the substrate may be run into thick building chemical-copper process to achieve thicknesses up to 8 μm . The flowchart in figure 3 describes the process steps.

Fig. 3 Process description.

IV. Experimental results

A. Dielectric formation

A compatible urethane is employed to form the dielectric on FR-4 substrate as seen in figure 5. The current process setting produces a 15 μm ayer thickness of the urethane. To increase the dielectric thickness to 30 μm , two layers have been spin-coated one after curing the other. The lamination process is performed by UV lamp.

B. Via hole formation

All via holes were drilled by 266 nm wavelength. The laser was tuned to outputs 3 mW and run through the square patterns according to table 2.

Fig. 4 Patterns used to form via holes.

Table. 2 Repetition times to form 20 and 10 μm via.

Dielectric thickness	Repetition
15 μm	6 times
30 μm	14 times

C. Via plating

A commercial Cu electroless plating process is used to plate copper on activated holes and pads. Figures 5 and 6 show the x-ray microtomography pictures for the obtained microvias for 20 μm and 10 μm as initial outer pattern diameter respectively.

Both samples uses 30 μm as dielectric thickness.

The samples demonstrate potential improvement for smaller via sizes by re-tuning the laser energy. The over size due to the via pad is controllable, by reducing the pad while activating the via holes.

Figure 7 illustrates the application of this process to real AlCu pad of a silicon chip. The pad has been tested to be conductive using daisy chain. To complement the point of supporting fan-out WLP, this full additive process has been employed to produce 5 μm wide copper traces on this urethane dielectric. Figure 8 illustrates this sample of 5 μm Cu traces.

Fig 5: Plated microvia with 20 μm initial outer pattern diameter.

Fig 6: Plated microvia with 10 μm initial outer pattern diameter.

Fig 7: Plated microvia to reach to AlCu pad of silicon chip.

Fig 8: 5 μm Cu traces on compatible urethane using the fully additive process.

V. Conclusion

Microvias of about 8 and 24 μm inner diameters on 30 μm thick dielectric have been demonstrated, using the 4th harmonic wavelength (266 nm) and a fully additive process.

It has also been demonstrated that the process is capable of producing 5 μm interconnects and also can be used to interconnect AlCu silicon chip pads.

The results of this work initiate further investigations to even smaller and well controlled sizes of below 10 μm . The factors to reconsider are the drilling power and repetition times. To remove the over size due to the via pad, one can set the activation area just equal to the via hole, on the other hand it can be challenging for our set-up where steps are not fully automated.

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