Chip-Coil Design for Wireless Power Transfer in Power Semiconductor Modules

Joakim Nilsson, Johan Borg, Jonny Johansson

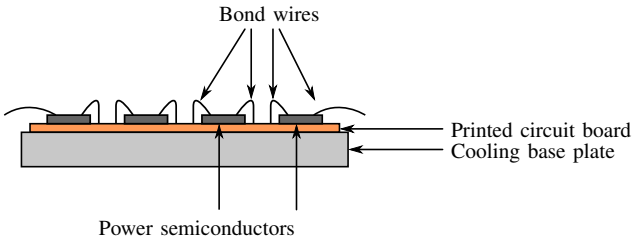

Fig. 1. Schematic view of the cross-section of a wire-bond power semiconductor module.

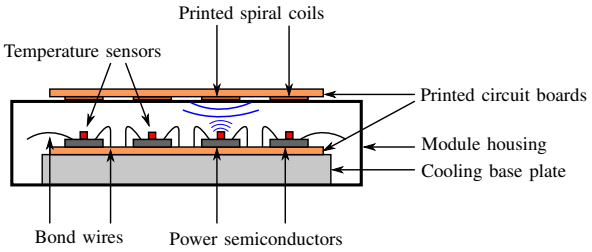

Fig. 2. Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by printed spiral coils mounted outside of the module.

***Abstract*—This paper presents electromagnetic simulations of a wireless power transfer system suitable for a monitoring system for detection of solder fatigue in power semiconductor modules. Power is provided wirelessly from a printed spiral coil on a printed circuit board to a silicon chip with an on-chip coil. We use and adapt a known gradient-ascent-based optimisation algorithm to obtain suitable coil geometries. For a frequency of 433 MHz, the simulations show an efficiency of -34.7 dB which we conclude is sufficient for the proposed monitoring system.**

***Index Terms*—CMOS coil, condition monitoring, low power, near-field, on-chip coil, RFID, power semiconductor, wireless**

I. Introduction

Solder faults in power semiconductor modules constitute a significant amount, $34\,\%$ of total failures in power electronic equipment [1]. It is thus desirable to monitor these faults so that they can be predicted and preventive maintenance can be performed before a failure occurs in order to avoid secondary or catastrophic failures. One way of predicting emerging faults is by monitoring the temperature of the power semiconductors [2]. A rise in temperature is an indication of emerging solder fatigue; voids forming in the solder interface between power semiconductor and base plate within a power semiconductor module, see Fig. 1 [3]. These voids reduce the cooling efficiency of the solder interface and may result in overheating and subsequent destruction of the power semiconductor device.

A wireless monitoring scheme for solder fatigue was proposed in [2] and is depicted in Fig. 2. Here, a radio-frequency identification (RFID) reader in the form of one or multiple printed spiral coils (PSCs) on a printed circuit board (PCB) communicate with and provide power to low-power (in the order of $10\,\mu\mathrm{W}$) temperature sensors with on-chip coils mounted on top of the power semiconductor devices. A wireless design has the advantage of providing galvanic isolation from the power semiconductors. Other advantages include that the system design becomes easily portable between power semiconductor modules, direct-contact of sensor with power semiconductor enables accurate measurements, and that no knowledge about the inner workings of the power semiconductor is required [2].

This paper presents the design methodology for, and the simulations of, a PSC coupled to an on-chip coil within a power semiconductor module. To design the coils with high power transfer efficiency and adequate output voltage, we used a slightly modified version of the algorithm presented by Zargham and Gulak in their work on coil design for biomedical implants [4]. The power transfer efficiency and output voltage demonstrated show that this algorithm can be used not only for implantable on-chip coils, but also for coils in power semiconductor modules.

This paper is organised as follows. In Section II we present the geometry of the propsed monitoring system. In Section III we present the optimisation algorithm with the simulation results in Section IV. In Section V we provide a discussion and comparison with other work and finally we provide a conclusion in Section VI.

II. Power Semiconductor Module Geometry

A schematic view of the geometry of a wire-bond power semiconductor module and a complementary metal-oxide semiconductor (CMOS) silicon chip as well as the different types of internal materials is shown in Fig. 3. Relevant parts of the monitoring system proposed in the introduction are also shown. The module housing is filled with a silicone dielectric gel. A ceramic substrate with power semiconductors soldered on top of it is attached onto a cooling base plate located at the bottom of the module. For our proposed monitoring system, temperature sensors are glued on top of the power semiconductors. In this work, we present simulations of two

978-1-5386-4221-4/18/$31.00

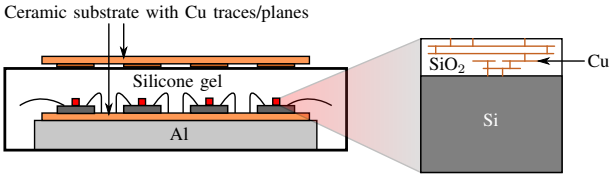

Fig. 3. Materials in the proposed monitoring system.

TABLE I
MATERIAL PROPERTIES FOR THE MATERIALS USED IN THIS WORK.

Material	**Rel. permittivity** (ε_r)	**Conductivity** (σ) [MΩ/m]
Silicon substrate	11.7	*not available**
Silicon dioxide	3.9	∼0
Silicone gel	2.1	∼0
FR-4	4.4	∼0
Copper	1	59.6

*Value known and used for simulations, but can not be published due to non-disclosure agreement.

coils, one PCB coil and one on-chip coil separated by $10\,\mathrm{mm}$ in a gel-filled power semiconductor module.

A. Chip Geometry

The bottom part of the temperature sensor chips consists of a lightly doped, p-type silicon substrate with low conductivity. The top part consists of a silicon oxide layer as well as copper traces. The process used in this work features 4 copper metal layers. Out of these four, the two top layers constitute the on-chip coil, shorted together with vias in the corners. Metal layer 2 (the second metal layer counting from the bottom) was not used at all for the coil and metal layer 1 was used as shielding from the conductive substrate. The shield consists of a chopped-up coil placed directly underneath the on-chip coil.

B. Material properties

Material properties for the materials used for the simulations of the proposed sensor system are presented in Table I. For all materials except for the silicone gel, the values are well-known. The relative permittivity, ε_r for the silicone gel was obtained by a capacitance measurement of the gel used in a common power semiconductor module.

III. Coil Geometry Optimisation

To implement the monitoring system proposed in the introduction, an inductive link between the PCB coils located on the outside of the power semiconductor module and the on-chip coils of sufficient power transfer efficiency must be designed. In this paper, we demonstrate how we use an optimisation algorithm, originally presented by Zargham and Gulak [4], to achieve a sufficiently high power transfer efficiency for our proposed monitoring system.

A. Simulation Model

A PSC is characterised by the following parameters: trace width, W; trace separation, S; coil outer dimension, d; and number of turns, N. An electromagnetic model for two coils separated by the media present in a power semiconductor module by a distance, D, was created. The electromagnetic simulator, FEKO [5], was used to evaluate the quality factors and power transfer efficiencies of these two coils. The model includes the media within the power semiconductor module, the materials and dimensions of a PCB as well as the materials and dimensions for a chip manufactured in a $0.35\,\mu\mathrm{m}$ CMOS process. To speed up simulation times, this model was simulated in 2.5D mode, where the dielectric materials presented in Table I were represented as infinite planes in the horizontal direction.

B. Algorithm

The algorithm used is similar to the one used in the work of Zargham and Gulak and for a detailed description we refer the reader to their work [4]. However, we present the psuedocode for our version of the algorithm in Table II.

The main differences between our algorithm and that of Zargham and Gulak is how we use frequency in our simulation and what is included in the power transfer efficiency, η.

1) Frequency: Zargham and Gulak continuously swept a range of frequencies in each iteration of the gradient ascent algorithm [4]. However, for our application it would be beneficial if the frequency was selected to lie within a frequency band where higher levels of radiated power are permitted. By using one of these bands, and if a sufficiently high power transfer efficiency is achieved, the radiated power may fall below the allowed maximum value without the need for the system to be shielded.

For our simulations, the optimisation algorithm was run on a set of select frequencies; namely $40.66\,\mathrm{MHz}$, $169.4\,\mathrm{MHz}$, $433.0\,\mathrm{MHz}$ and $868.0\,\mathrm{MHz}$. The frequencies are chosen to lie within the industrial, scientific and medical (ISM) bands recommended by International Telecommunications Union (ITU) [6] and the frequency bands recommended by the Swedish Post and Telecom Authority (PTS) [7].

2) Power Transfer Efficiency: The other difference comes down to what is included in the power transfer efficiency, η. Zargham and Gulak optimised for a power transfer efficiency for a 2-port network with the assumption that the network is driving an optimal load [4]. Such a load can theoretically be realised using matching networks, but for on-chip coils and especially for light loads, large inductances would be required. Thus, the matching inductor may not be practical to manufacture on-chip with sufficiently high quality factors.

When evaluating the power transfer efficiency, we only include a single capacitor in the on-chip matching network. It has been estimated earlier that for a temperature monitoring system, $10\,\mu\mathrm{W}$ will be sufficient [8]. Therefore we assumed a $100\,\mathrm{k}\Omega$ load for our simulations because such a load would consume $10\,\mu\mathrm{W}$ at a supply voltage of $1\,\mathrm{V}$.

IV. Simulation Results

The algorithm presented in Table II was run for the following frequencies: $40.66\,\mathrm{MHz}$, $169.4\,\mathrm{MHz}$, $433.0\,\mathrm{MHz}$ and $868.0\,\mathrm{MHz}$ for a coil separation, $D = 10\,\mathrm{mm}$. Out of

TABLE II
POWER TRANSFER EFFIIENCY OPTIMISATION ALGORITHM FOR COIL GEOMETRIES

step 1: initialisation

$N_{\text{pcb}} := 2$
$W_{\text{pcb}} :=$ minimum allowed PCB width
$S_{\text{pcb}} :=$ minimum allowed PCB spacing
$d_{\text{pcb}} := D \cdot \sqrt{2(1+\sqrt{5})}$

$N_{\text{chip}} := 2$
$W_{\text{chip}} :=$ minimum allowed chip width
$S_{\text{chip}} :=$ minimum allowed chip spacing
$d_{\text{chip}} :=$ chip die size

step 2: PCB coil quality factor optimisation

for $2 \leq N_{\text{pcb}} \leq 5$:
  gradient ascent algorithm:
    search: N_{pcb}, W_{pcb}, S_{pcb}
    maximise: Q
update: N_{pcb}, W_{pcb}, S_{pcb} for maximum Q

step 3: on-chip coil quality factor optimisation

for $2 \leq N_{\text{chip}} \leq 5$:
  gradient ascent algorithm:
    search: N_{chip}, W_{chip}, S_{chip}
    maximise: Q
update: N_{chip}, W_{chip}, S_{chip} for maximum Q

step 4: PCB-coil-based power transfer efficiency optimisation

for $2 \leq N_{\text{pcb}} \leq 5$:
  gradient ascent algorithm:
    search: N_{pcb}, W_{pcb}, S_{pcb}, d_{pcb}
    maximise: η
update: N_{pcb}, W_{pcb}, S_{pcb}, d_{pcb} for maximum η

step 5: on-chip-coil-based power transfer efficiency optimisation

for $2 \leq N_{\text{chip}} \leq 5$:
  gradient ascent algorithm:
    search: N_{chip}, W_{chip}, S_{chip}
    maximise: η
update: N_{chip}, W_{chip}, S_{chip} for maximum η

step 6: stop condition

if η improved since step 4:
  go to step 4
else:
  stop

those frequencies, the optimisation algorithm yields the best results for $433\,\text{MHz}$, so in this section the results of simulations for $433\,\text{MHz}$ are presented. A $2.0 \times 2.0\ \text{mm}^2$ integrated circuit (IC) design for a $0.35\,\mu\text{m}$ process with the dimensions obtained from the simulations presented in this work has been submitted for fabrication.

For the on-chip coil, the simulation algorithm yields the highest power transfer efficiency for a trace width of $48\,\mu\text{m}$. However, the design rules the $0.35\,\mu\text{m}$ used do not allow such wide traces, thus the trace width was adjusted to $35\,\mu\text{m}$ with only a minor impact on power transfer efficiency. Furthermore, while the algorithm calculated a trace separation of $0.6\,\mu\text{m}$, theoretical calculations revealed that the major capacitance contribution comes from the coil and not from the on-chip

TABLE III
COIL GEOMETRIES OPTIMISED FOR $433\,\text{MHz}$

Parameter		**PCB coil**	**On-chip coil**
Trace width,	W	$3500\,\mu\text{m}$	$35\,\mu\text{m}$
Trace seperation,	S	$840\,\mu\text{m}$	$6.0\,\mu\text{m}$
Outer dimension,	d	$25.4\,\text{mm}$	$2.0\,\text{mm}$
No. of turns,	N	2	5

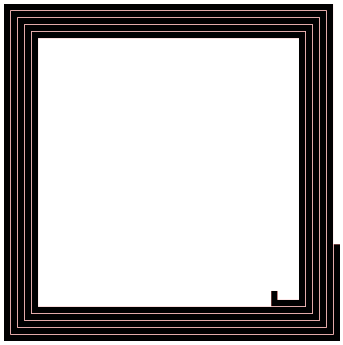

Fig. 4. Chip coil with the dimensions specified in Table III.

capacitor for such a small trace separation. This may pose a problem to achieve the desired resonant frequency if the process parameters are not modelled accurately enough. Therefore, this value was adjusted to $6.0\,\mu\text{m}$ and the value for the on-chip capacitor was recalculated. For the adjusted geometry, the on-chip capacitor, which is known to a greater accuracy compared to the coil capacitance, is the major contributor for capacitance. These adjustments reduced the power transfer efficiency by $0.5\,\text{dB}$. The final dimensions for both PCB and on-chip coil are presented in Table III, while an image of the resulting chip coil is presented in Fig. 4. Using those parameters for our simulations as well as an on-chip, parallel $1.20\,\text{pF}$ capacitor yields a power transfer efficiency of $-34.7\,\text{dB}$. The PCB coil's outer dimension of $25.4\,\text{mm}$ makes it sufficiently small to fit on top of most power semiconductor modules.

For comparison, the resulting power transfer efficiencies for the initial simulations, without adjusted geometries, for different frequencies are presented in Table IV.

V. DISCUSSION

The simulation results presented in Section IV show that it is possible to achieve power transfer efficiencies which are high enough to power the low-power monitoring system presented in the introduction. However, comparing the power transfer efficiency of this work, $-34.7\,\text{dB}$, with the power transfer efficiency of the work of Zargham and Gulak [4], who achieve a measured power transfer efficiency of $-20.15\,\text{dB}$ at $187\,\text{MHz}$ through $10\,\text{mm}$ of bovine muscle reveals that other systems

TABLE IV
POWER TRANSFER EFFICIENCIES FOR INITIAL SIMULATIONS AT DIFFERENT FREQUENCIES

Frequency [MHz]	40.66	169.4	433.0	868.0
Power transfer efficiency [dB]	-61.4	-41.4	-34.2	-37.6

978-1-5386-4221-4/18/$31.00 ©2018 IEEE

can achieve higher power transfer efficiencies. In this section, we compare our results with those of [4] and comment on power transfer efficiency in general. The authors are not aware of other wireless power transfer systems for CMOS ICs which achieve similar power transfer efficiencies to those of Zargham and Gulak.

A. Conductive Media and Frequency

The intended application for the work of Zargham and Gulak is implantable chips in humans for medical purposes. Thus they report power transfer efficiencies through bovine muscle, which is more conductive than the silicone gels found in power semiconductor modules, which are insulators. As this conductivity increases with frequency, so do the conductive losses which explains the fact that our simulations resulted in a higher operating frequency than that of Zargham and Gulak. Another difference between the two works is that Zargham and Gulak allowed any operating frequency while we required for our work that the operating frequency lie within an ISM band. This requirement has both advantages and disadvantages. The obvious advantage of having the operating frequency in an ISM band is that the allowed radiated power is high compared to other bands and the requirement to shield the system may thus be removed. Another advantage is that the simulation time can be significantly reduced if the simulations need only to be carried out for select frequencies in contrast to be swept over a range of frequencies. A disadvantage is that limiting the available frequencies reduces the power transfer efficiency unless the optimal frequency occurs within an ISM band.

B. Low-power Operation

Zargham and Gulak evaluates power consumption assuming that a matching network can be designed which allows the wireless power transfer system to drive an optimal load. For our system we have assumed a $100\,\mathrm{k\Omega}$ load, which is suitable if our proposed temperature monitoring system was to be realised. This limits the achievable power transfer efficiency because of the matching components required to drive such a load with optimal efficiency. Thus, we have evaluated the power transfer efficiency using only a capacitor in parallel to the load as a matching network. The possibility to manufacture components to drive an optimum load on a CMOS chip would have significantly increased the power transfer efficiency.

C. Power Transfer Efficiency

The total power transfer efficiency, η, can be divided into several components of power transfer efficiencies. The power transfer efficiency can be written as

$$\eta = \eta_{\text{source}} \cdot \eta_{\text{link}} \cdot \eta_{\text{matching}} \cdot \eta_{\text{rectifier}}, \tag{1}$$

where η_{source} is the power transfer efficiency of the power amplifier driving the PCB coil; η_{link} is the power transfer efficiency due of the wireless link and includes losses in the media between the coils, the power lost due to radiation as well as the power lost due to resistive heating in the coils; η_{matching} is the power transfer efficiency of the matching network; and $\eta_{\text{rectifier}}$ is the power transfer efficiency of a rectifier placed before the load.

In this work, we have focused on optimising $\eta_{\text{link}} \cdot \eta_{\text{matching}}$ as these are the major contributors to losses for wireless power transfer systems to ICs. [9] has demonstrated a class E power amplifier with a power transfer efficiency of $89.5\,\%$ at $450\,\mathrm{MHz}$, while [10] has demonstrated an active rectifier with a power transfer efficiency of $53.5\,\%$ at $100\,\mathrm{MHz}$ while arguing that it should be possible to design a rectifier with a power transfer efficiency of over $70\,\%$ for frequencies up to $600\,\mathrm{MHz}$ if certain challenges are overcome.

VI. Conclusion

In this paper we present simulations which demonstrate a power transfer efficiency of $-34.7\,\mathrm{dB}$ for a wireless power transfer system within a power semiconductor module constituting a transmitter PCB PSC to a receiver CMOS PSC separated by $10\,\mathrm{mm}$. The intended application is a temperature monitoring system for power semiconductor modules which would enable the detection of emerging faults such as solder fatigue. The simulations show that it is feasible to construct a wireless power transfer system which provides sufficient power for a low-power CMOS temperature sensor to operate, such as the one demonstrated in [8]. For example, if $10\,\mu\mathrm{W}$ is required for the sensor, approximately $30\,\mathrm{mW}$ would have to be input to the wireless power transfer system. Taking into account the power transfer efficiencies of state-of-the-art high-frequency power amplifiers and rectifiers, approximately $62\,\mathrm{mW}$ would have been required.

References

[1] E. Wolfgang, "Examples for failures in power electronics systems," *ECPE tutorial on reliability of power electronic systems, Nuremberg, Germany*, 2007.

[2] J. Nilsson, J. Borg, and J. Johansson, "Single chip wireless condition monitoring of power semiconductor modules," in *Nordic Circuits and Systems Conference (NORCAS): NORCHIP International Symposium on System-on-Chip (SoC), 2015*, Oct 2015, pp. 1–4.

[3] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, vol. 1, May 1997, pp. 425–430 vol.1.

[4] M. Zargham and P. Gulak, "Fully integrated on-chip coil in 0.13 µm CMOS for wireless power transfer through biological media," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 9, no. 2, pp. 259–271, April 2015.

[5] FEKO, *version 7.10.0 (R2010a)*. EM Software and Systems-S.A. (Pty) Ltd, 2015.

[6] International Telecommunications Union, *Radio Regulations, Chapter 1*, Std., 2016.

[7] Swedish Post and Telecommunications Authority, *Frekvensplan MHz*, Std., 2012. [Online]. Available: http://www.pts.se/upload/Remisser/2009/Frekvensplan-MHz.pdf

[8] J. Nilsson, J. Borg, and J. Johansson, "High-temperature characterisation and analysis of leakage-current-compensated, low-power bandgap temperature sensors," *Analog Integrated Circuits and Signal Processing*, Jun 2017. [Online]. Available: https://doi.org/10.1007/s10470-017-1011-6

[9] Y.-O. Yam and C.-W. Cheung, "High efficiency power amplifier with travelling-wave combiner and divider," *International journal of electronics*, vol. 82, no. 2, pp. 203–218, 1997.

[10] J. Fischer, J. Borg, and J. Johansson, "High frequency limitations of active rectifier circuits for RFID applications," in *2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems*, June 2016, pp. 326–329.

978-1-5386-4221-4/18/$31.00 ©2018 IEEE