Feasibility analysis of specialized PEEC solvers in comparison to SPICE-like solvers

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Abstract The Partial Element Equivalent Circuit (PEEC) method provides an electric equivalent circuit for a physical geometry. This circuit can be combined with external passive/active lumped elements, enabling the simulation and co-design of combined circuit and electromagnetic (EM) structures. The resulted circuit can be solved in a dedicated solver, or equivalently can be exported to a SPICE-like solver. In this paper, the inclusion of passive and active lumped circuit elements in PEEC method has been studied and a combined solver has been developed. To demonstrate the capability of the solver, three structures are examined. All examples include a transmission line-PEEC model and active components. Results are compared with those from OrCAD, where an analytical model for the transmission line is used. Good agreement between the results shows the feasibility of using PEEC to solve this type of mixed problems. Also, comparison has been made in terms of implementation and feasibility for the aim of developing the optimal EM solver with active elements support. It is shown that SPICE is not a suitable choice to solve the PEEC models and, a specialized solver can solve the system in a much faster way. On the other hand, all the definitions and models of circuit devices e.g. transistors, MOSFETs, etc. should be implemented in the specialized solver, which raises a trade-off between the solution time and the implementation time.

Keywords Partial element equivalent circuit (PEEC) method · Non-linear circuit elements · Combined circuit/electromagnetic simulation

1 Introduction

By moving toward higher frequencies every wire, joint, and bondwire acts an antenna, and radiation and coupling effects play an important role in the system behavior. Packaging, orientation of wires and components, selection of dielectric substrate, and other structural parameters in the PCB assembly all affect the performance of the system, and should be considered in the design of new products. In all the situations, simulation techniques where both the EM structures and lumped passive/active elements can be incorporated are desired. To cope with the new challenges, various techniques have been applied to different EM numerical methods.

A considerable effort has been made to incorporate lumped elements into the Finite-Difference Time-Domain (FDTD) method. The so-called lumped-element FDTD (LE-FDTD) method can be used to include single resistors, capacitors, inductors, diodes, and transistors directly in the EM simulation [1]. When the method suffers from inaccuracies and heavy CPU computations, implementing complex models for diodes and transistors, specifically non-linear capacitors, is an issue [2]. Another limitation of this technique is that it cannot easily and accurately model complex and arbitrary networks of lumped elements [2]. Furthermore, the hybrid FDTD-SPICE method has been proposed to incorporate more general circuits, where programming the link between FDTD and SPICE can be time consuming [3]. The third approach proposed in the literature is called lumped-network FDTD (LN-FDTD), in which the RLC lumped network is described in terms of its impedance in the Laplace domain. The resulted equation is then fitted into FDTD algorithm by using digital signal-processing techniques [2].

Similar to FDTD, studies are performed to incorporate lumped elements into the Finite-Element Time-Domain (FETD) method by direct stamping of the voltage-current

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relationships into the finite element matrices [4, 5]. These methods are not flexible when dealing with complex networks of lumped elements. Also conditional stability imposes a very small time step requirement in order to converge to a final solution.

The PEEC method [6] is a numerical method which is based on an integral form of Maxwell's equations and proposes an equivalent circuit for a mixed conductor/dielectric structure. Resistive, capacitive and inductive properties of each cell in the structure is represented as resistance, (partial) coefficients of potential [7] and partial inductance [8] respectively. Also, the electric and magnetic couplings between the cells are implemented as mutual capacitances and mutual partial inductances [6]. Since the method is extracted from an integral form of Maxwell's equations, the free space discretization will not be performed, which makes PEEC a suitable method for applications where the structure is not bounded, for example some classes of EMC problems. The first part of the method involves discretization of the structure and calculating the equivalent circuit, and the second part is basically a circuit solver, where by writing the Kirchhoff's voltage and current laws (KVL and KCL) for the equivalent circuit, a system of linear equations is acquired. This system can be solved to obtain the potential and current distributions in the structure [9]. Inclusion of passive lumped elements can be easily obtained by appending the linear current-voltage (I - V) relation for the element to the PEEC system of equations. Active lumped elements on the other hand introduce non-linear equations to the system where the Taylor's expansion method can be applied to linearize the equations. This technique requires no change to the discretized cell structure or applied boundary conditions, and implementing any active components can be done only by modifying the circuit solver and including the component definitions and equations into the solver.

There are two obvious routes to combine PEEC and SPICE (circuit) problems. The first is by bringing the PEEC models into an existing SPICE-like solver [10]. Wollenberg *et al.* utilized this approach by modifying an open source SPICE-solver to include PEEC models [10]. The drawback is the solution time that quickly increases for the combined solver since SPICE-like solvers are optimized for solving circuit equations and not the fully coupled systems arising from PEEC models. The second option is to bring SPICE models into a dedicated PEEC-solver [11]. In this paper, a dedicated PEEC-solver is developed, and theoretical and technical issues are discussed. The dedicated solver comprises two solvers. The first one is a PEEC solver which reads the physical specifications of an EM problem (including dimensions, conductivity, meshing, etc.) and extracts the equivalent circuit. The second solver is technically a circuit solver which reads a standard SPICE input file (.cir file) including all linear/non-linear lumped circuit elements, and

appends them to the PEEC equivalent circuit and finally solves the whole system in time. Three test cases are examined to test the reliability of the dedicated solver and good agreement between the results are obtained. The drawback of this approach is that all SPICE-models have to be implemented in the dedicated PEEC-solver. On the other hand, a noticeable time difference exists between the solution time of this solver and SPICE-like solvers. By studying the size, sparsity and the pattern of the matrices, along with the solution time of the PEEC-solver and SPICE, it is shown that the solution time of SPICE-like solver drastically increases as the size of the equivalent circuit increases, while the dedicated PEEC-solver simulates the structures in a more reasonable time. The time comparisons to some extent shows the trade-off between the implementation time, and the solution time of both approaches.

This paper starts with a brief introduction to the PEEC method in Sect. 2. In Sect. 3, Modified Nodal Analysis for both PEEC and SPICE in quasi-static form are introduced and compared. The systems of equations are extracted for a simple example and matrix size difference is presented. Incorporating external lumped elements in the system of equations has been studied in Sect. 4. Linearization of p-n junction diode equations has been investigated and the Newton-Raphson (NR) algorithm to solve the *linearized* system is introduced. In Sect. 5, three test cases including a diode and BJTs have been studied and comparison has been made between the results of the PEEC solver and the results of a commercial circuit solver OrCAD in order to check the reliability of the developed solver. Finally in Sect. 6, solution time of the PEEC-solver and the SPICE-solver for different problem sizes are compared in order to study the feasibility of each solver to handle EM problems combined with passive/active circuit elements. Comparisons are made for two cases when linear and non-linear components exist in the circuit.

2 The PEEC method

The approach starts with writing the summation of electric field at a conductor in free space [9] according to

$$\mathbf{E}_0(\mathbf{r}, t) = \frac{\mathbf{J}(\mathbf{r}, t)}{\sigma} + \frac{\partial \mathbf{A}(\mathbf{r}, t)}{\partial t} + \nabla \Phi(\mathbf{r}, t) \quad (1)$$

where $\mathbf{E}_0$ is an external electric field, $\mathbf{J}$ is the current density flowing in the conductor, $\mathbf{A}$ is the magnetic vector potential, and Φ is the scalar potential. The vector and scalar potentials at any point are given by

$$\mathbf{A}(\mathbf{r}, t) = \mu \int_{v'} G(\mathbf{r}, \mathbf{r}') \mathbf{J}(\mathbf{r}', t_d) dv' \quad (2)$$

$$\Phi(\mathbf{r}, t) = \frac{1}{\epsilon} \int_{S'} G(\mathbf{r}, \mathbf{r}') q(\mathbf{r}', t_d) dS' \quad (3)$$

where c is the speed of light, t_d is the retardation time, q is the charge density, and G is the Green's function for free space [6, 9]. Substituting (2) and (3) into (1) the following integral equation [12] will result

$$E_0(\mathbf{r}, t) = \frac{\mathbf{J}(\mathbf{r}, t)}{\sigma} + \frac{\mu}{4\pi} \int_{v'} \frac{1}{|\mathbf{r} - \mathbf{r}'|} \frac{\partial \mathbf{J}(\mathbf{r}', t_d)}{\partial t} dv' + \frac{1}{4\pi\epsilon} \int_{S'} \frac{1}{|\mathbf{r} - \mathbf{r}'|} q(\mathbf{r}', t_d) dS' \quad (4)$$

To solve this integral equation, the structures are discretized into volume cells and surface cells where the current densities and charge densities are considered uniformly distributed in each volume cell and over each surface cell respectively [6]. Therefore the current density $\mathbf{J}$ and charge density q can be taken out of the integrals. By applying the Galerkin's method and taking the volume integral from (4) over each of the volume cells, and also using the definitions of partial inductance [8] and coefficients of potential [7], (4) can be written as a system of Neutral Delay Differential Equations (NDDE). The resulting system of NDDEs is in the following form [12, 13]

$$C_0 y'(t) + G_0 y(t) + C_1 y'(t - \tau) + G_1 y(t - \tau) = Bu(t, t - \tau) \quad (5)$$

where the C_0 , G_0 , C_1 , G_1 and B are real-valued matrices and the retarded couplings (τ) must be interpreted in an operator sense. In quasi-static situations where retardation is small and can be ignored, the NDDE system will be reduced to a system of Ordinary Differential Equations (ODE) and can be written in matrix form as follows [13, 14]

$$\begin{bmatrix} -\Pi & -(R + L_p \frac{d}{dt}) \\ P^{-1} \frac{d}{dt} & \Pi^T \end{bmatrix} \begin{bmatrix} \Phi \\ I_L \end{bmatrix} = \begin{bmatrix} V_s \\ I_s \end{bmatrix} \quad (6)$$

where R is resistance matrix, L_p is the matrix of coefficients of partial inductances [8], and P is the matrix of coefficients of potentials [7]. Π is the connectivity matrix and describes the connections between volume cells and surface cells [13]. V_s and I_s are source vectors and Φ and I_L are the potentials of the surface cells and currents through volume cells, respectively. This formulation will be referred to as MNA (Modified Nodal Analysis) formulation later on [15].

By defining a proper *time step* and using an integration technique, for example the Backward-Euler approximation [16] for its stability [14], for the time derivatives $\frac{\partial}{\partial t}$, the system of (6), also referred to as $Ax = b$, can be solved in time. At each time step, the sources, b , are simply updated and the system is solved to obtain the node potentials and volume cell currents at that time step.

Fig. 1 Zero thickness bar (top view)

Fig. 2 PEEC equivalent circuit

3 Modified nodal analysis for PEEC models in a dedicated PEEC solver and SPICE

3.1 Formulation in a dedicated PEEC solver

In this section, a MNA formulation of a simple PEEC model is presented. For this purpose, a metallic bar, shown in Fig. 1(a), is discretized into two volume cells and three surface cells. The volume cells and surface cells are presented in Figs. 1(b) and 1(c) respectively. Nodes are numbered from 1 to 3. Currents flowing through the volume cells are assumed to be uniform, and are labeled I_1 and I_2 . The quasi-static equivalent circuit for this structure is plotted in Fig. 2. V_1 , V_2 , and V_3 represent the potentials of the surface cells Φ_1 , Φ_2 , Φ_3 in Fig. 1(c) respectively. This notation is adopted

for the potentials to comply with the circuit analysis literature. Capacitors model the electric coupling between the surface cells, and the mutual inductors account for the magnetic couplings between the volume cells. Resistances of the volume cells are modeled by R_{11} and R_{22} . Capacitance values can be calculated directly from the P matrix. The MNA formulation for this structure composes of two KVL relations and three KCL relations, as shown in (7). KVLs are written for RL branches (from node 1 to node 2, and from node 2 to node 3). KCLs are written only at nodes 1, 2, and 3. KVL for other branches and KCL at other nodes are not directly formulated in MNA matrix, e.g. the currents through C_{12} , C_{13} , and C_{23} are not treated as unknowns in the system, but

they are included in (7) based on their relations to voltages at nodes 1, 2, and 3. Also, by taking advantage of the PEEC model structure, no KCL is written for the nodes between the inductors and resistors in RL branches. For example, by looking at the RL branch consisting of the resistor R_{11} and the inductor L_{11} , it can be seen that the current through R_{11} and the current through L_{11} are the same and equal to I_1 and therefore there is no need to write a KCL at the node between the two components. Thus, the PEEC-MNA formulation for this circuit only consists of five unknowns. The first two rows in (7) represent the KVLs and the next three rows show the KCL relations.

$$\begin{bmatrix} +1 & -1 & 0 & -R_{11} - L_{11} \frac{d}{dt} & -L_{12} \frac{d}{dt} \\ 0 & +1 & -1 & -L_{12} \frac{d}{dt} & -R_{22} - L_{22} \frac{d}{dt} \\ (C_{11} + C_{12} + C_{13}) \frac{d}{dt} & -C_{12} \frac{d}{dt} & -C_{13} \frac{d}{dt} & +1 & 0 \\ -C_{12} \frac{d}{dt} & (C_{12} + C_{22} + C_{23}) \frac{d}{dt} & -C_{23} \frac{d}{dt} & -1 & +1 \\ -C_{13} \frac{d}{dt} & -C_{23} \frac{d}{dt} & (C_{13} + C_{23} + C_{33}) \frac{d}{dt} & 0 & -1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (7)$$

3.2 Formulation in SPICE/ORCAD

If a circuit contains $N + 1$ nodes (including the ground node) and N_v voltage-defined branches (e.g. inductors, voltage sources, etc.), then the N node voltages and the N_v voltage-defined branch currents become the unknown circuit variables in the SPICE-MNA formulation [16, 17]. The SPICE-MNA formulation for the same circuit (Fig. 3) is shown in (8). The voltages at nodes 1 to 5 and the currents through the inductors I_1 and I_2 are defined as unknowns. The first

two rows in (8) represent KVLs for inductors L_{11} and L_{22} , and including the mutual coupling between them. The next five rows show the KCLs at nodes 1 to 5 where the currents through the resistors and capacitors are expressed based on their node voltages. For example, the KCL at node 1 includes $C_{11} \frac{dV_1}{dt}$ for the current through C_{11} , $C_{12} \frac{d(V_1 - V_2)}{dt}$ for the current through C_{12} , $C_{13} \frac{d(V_1 - V_3)}{dt}$ for the current through C_{13} , and I_1 as the current through the inductor L_{11} . It can be seen that the matrix size has increased to 7×7 .

$$\begin{bmatrix} 1 & 0 & 0 & -1 & 0 & L_{11} \frac{d}{dt} & L_{12} \frac{d}{dt} \\ 0 & 1 & 0 & 0 & -1 & L_{12} \frac{d}{dt} & L_{22} \frac{d}{dt} \\ (C_{11} + C_{12} + C_{13}) \frac{d}{dt} & -C_{12} \frac{d}{dt} & -C_{13} \frac{d}{dt} & 0 & 0 & 1 & 0 \\ -C_{12} \frac{d}{dt} & (C_{12} + C_{22} + C_{23}) \frac{d}{dt} + \frac{1}{R_{11}} & -C_{23} \frac{d}{dt} & -\frac{1}{R_{11}} & 0 & 0 & 1 \\ -C_{13} \frac{d}{dt} & -C_{23} \frac{d}{dt} & (C_{13} + C_{23} + C_{33}) \frac{d}{dt} + \frac{1}{R_{22}} & 0 & -\frac{1}{R_{22}} & 0 & 0 \\ 0 & -\frac{1}{R_{11}} & 0 & \frac{1}{R_{11}} & 0 & -1 & 0 \\ 0 & 0 & -\frac{1}{R_{22}} & 0 & \frac{1}{R_{22}} & 0 & -1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (8)$$

Fig. 3 SPICE equivalent circuit

4 External circuit components

In the previous sections, the PEEC method and the way it models an electromagnetic structure (geometry) as an equivalent circuit was introduced. Also the MNA-formulation of PEEC models in both, a dedicated solver, and SPICE were studied. In this section it is assumed that external lumped circuit elements (e.g. resistors, capacitors, diodes, etc.) are connected to this geometry, and the way these linear/non-linear components are modeled and how they are formulated in the PEEC-MNA formulation is investigated.

4.1 Linear components

Linear components can easily be formulated in the MNA matrix by “stamping” [16] and no extra work is needed to solve the MNA system. KVL relation is written for the component and KCLs at proper nodes (the nodes that the component is connected to) are updated in the MNA formulation.

A resistor R_1 connected between nodes i and j introduces one new unknown, which is the current flowing through that resistor (I_{R_1}). This unknown should be appended to the unknowns vector $\mathbf{x}$. The KVL for the resistor $V_i - V_j = RI_{R_1}$ adds a new row to the matrices A and b , where the corresponding row of the source vector b for this equation obviously is zero. The next step is to modify the KCL relations for nodes i and j with respect to the current direction adopted in R_1 .

For linear capacitors and inductances, the equation relating the current flowing through the component and the voltage across it is in the form of a differential equation. Trapezoidal integration method is used to transform this differential equation into a linear algebraic form. This method is more accurate compared to Backward-Euler integration

method and it is the default numeric integration algorithm used in SPICE [16, 18]. For example, the I - V relation for the capacitor [19] can be written as

$$V_c(t+1) - \frac{dt}{2C} I_c(t+1) = V_c(t) + \frac{dt}{2C} I_c(t) \quad (9)$$

To implement a capacitor connected between nodes i and j in the MNA formulation, the capacitor current I_c is defined as a new unknown in vector $\mathbf{x}$, KCL is updated for these nodes with respect to the current direction in the capacitor, and finally a new row is appended to matrices A and b . The row in A implements the left hand side of (9) and the corresponding row in b contains the right hand side of this equation, updated at each time point.

4.2 Non-linear components

Implementing non-linear components is slightly more complicated than linear components. Non-linear components are defined by their I - V relationships which change in response to the DC bias of the component. Since the system equations represent linear relationships, non-linear components become a problem [18]. To solve this problem, the non-linear I - V relations of these components has to be linearized [16, 18, 19].

4.2.1 Diode

The diode current I_D in terms of diode voltage V_D in direct bias is given [20] by

$$I_D(V_D) = I_s \left(e^{\frac{V_D}{nV_T}} - 1 \right) \quad (10)$$

in which $V_T = \frac{kT}{q}$, n is the emission coefficient, k is the Boltzmann constant, T is the absolute temperature and q is the electron charge. This non-linear equation should be modified and linearized in order to be put in the MNA matrix formulation. For this purpose, the non-linear equation is expanded using Taylor's series around an arbitrary value of $V_D = V_{D0}$. The Taylor's expansion for an arbitrary equation $f(x) = 0$ around x_k [19] is in the following form

$$f(x_{k+1}) = f(x_k) + f'(x_k)(x_{k+1} - x_k) + \frac{1}{2} f''(\xi)(x_{k+1} - x_k)^2 \quad (11)$$

where $(x_k \leq \xi \leq x_{k+1})$ and $f'''(\xi)$ should exist over that entire interval as well. Using this equation for the diode current and ignoring the second order term results in

$$I_D(V_D) \approx I_D(V_{D0}) + (V_D - V_{D0}) I_D'(V_{D0}) \\ = I_s \left(e^{\frac{V_{D0}}{nV_T}} - 1 \right) + (V_D - V_{D0}) \frac{I_s}{nV_T} e^{\frac{V_{D0}}{nV_T}}. \quad (12)$$

Rearranging (12) will result in the following equation

$$I_D = G_{eq} V_D + I_{eq} \quad (13)$$

in which

$$I_{eq} = I_s (e^{\frac{V_{D0}}{nV_T}} - 1), \quad \text{and} \quad (14a)$$

$$G_{eq} = \frac{I_s}{nV_T} e^{\frac{V_{D0}}{nV_T}}. \quad (14b)$$

Equation (13) is a linearized form of (12) and can be used in the MNA formulation. However, unlike the case of linear components, where potentials and currents at each time point are calculated in a single step, an iterative procedure (known as Newton-Raphson algorithm) [16, 18, 19] should be used at each time point for the non-linear components. The Newton-Raphson algorithm is described below:

At each time point t_{k+1} ,

1. Make an initial guess for each potential and current ($\mathbf{x}_k$).
2. Linearize all non-linear equations based on $\mathbf{x}_k$ (e.g. $G_{eq,k}$ and $I_{eq,k}$ for each diode is calculated and (13) is updated respectively).
3. Build matrices A_k and b_k based on all linear and linearized equations.
4. Solve the system $A_k \mathbf{x}_{k+1} = b_k$ to calculate $\mathbf{x}_{k+1}$.
5. If $|\mathbf{x}_k - \mathbf{x}_{k+1}| < \epsilon_a + \epsilon_r |\mathbf{x}_{k+1}|$, the solution has converged and $\mathbf{x}_{k+1}$ is the solution for this time point, otherwise replace the previous initial guesses with current solution, i.e. $\mathbf{x}_k = \mathbf{x}_{k+1}$ and go to step (2).

In transient analysis, the initial guess at each time point is the solution at the previous time point, and the initial guess for the first time point $\mathbf{x}_0$ is the DC solution of the circuit.

Two constants, an *absolute error tolerance* ϵ_a and a *relative error tolerance* ϵ_r , are introduced to check the convergence criterion. These error tolerances are important in first to determine the accuracy of the Newton-Raphson algorithm and second, to define the number of iterations required to find the solution [18].

The *relative error tolerance* is used to maintain the ratio $|\mathbf{x}_k - \mathbf{x}_{k+1}|/|\mathbf{x}_{k+1}|$ below a certain level ($\mathbf{x}_k$ and $\mathbf{x}_{k+1}$ are potential/current values in two successive iterations). On the other hand, in case the potential/current approaches zero, the relative error, $|\mathbf{x}_k - \mathbf{x}_{k+1}|$, approaches zero, which means the results are infinitely accurate. To avoid such situations, *absolute error tolerances* are introduced. They set an upper limit for the difference between the values of potentials or currents in successive iterations [16, 18].

As a convergence aid, a small conductance G_{min} is placed in parallel to each PN junction of every semiconductor model in SPICE [16, 18] (default value of this conductance is $10^{-12} \Omega$). This conductance prevents the Newton-Raphson algorithm to fail under conditions where the component conductance becomes zero (when the I - V curve has zero slope, as in ideal diode in reverse bias).

Another source of divergence in the Newton-Raphson algorithm is discontinuities in component models [18]. For most of non-linear components, different regions of operation are defined by different equations. Therefore, the Newton-Raphson algorithm can diverge when the component is operating close to model discontinuity [18]. Newton-Raphson algorithm might switch (oscillate) between these regions in successive iterations without leading towards the solution. To eliminate this issue, care must be taken while modeling the non-linear components. Here the diode model from NGSPICE [21] is used where equations and their derivatives in different regions of operation are continuous. The diode equations for different regions of operation are

$$I_D = \begin{cases} I_s (e^{\frac{V_D}{nV_T}} - 1) + G_{min} V_D, & V_D > -3V_T \\ -I_s (1 + (\frac{3V_T}{e^{1.0}} V_D)^3) + G_{min} V_D, & V_D > -V_{brk} \\ -I_s (e^{\frac{V_{brk} + V_D}{nV_T}} - 1 + \frac{V_{brk}}{V_T}) + G_{min} V_D, & \text{otherwise} \end{cases} \quad (15)$$

where V_{brk} is absolute value of the *Break-down voltage* of the diode.

4.2.2 Bipolar junction transistor (BJT)

Bipolar Junction Transistors (BJTs) can be modeled as two interacting *pn* junction diodes. Depending on the status of each of these diodes, four operating regions can be defined for BJTs, e.g. normal active region, saturated region, inverse region, and off region, and based on the operating region of the BJT, the relations for collector current I_C and base current I_B change. The model used here is called Ebers-Moll model [20], which is presented in Fig. 4. The current-dependent current source models the coupling between two junctions. Three small resistors r_c , r_b , and r_e are also included in the model, which improve the dc characterization of the model. They represent the ohmic resistance of the terminals of the transistor [20] (not shown in the model in Fig. 4).

The implementation of the BJT in the MNA formulation is basically the same as for a diode. The Newton-Raphson algorithm should be used to find the operating point of the BJT at each time point.

4.2.3 Non-linear capacitors

To account for charge-storage effects in junction diodes and bipolar junction transistors, non-linear capacitors are included in the component models. Without these capacitors, the component would be infinitely fast. The charge stored in

these non-linear capacitors changes as a function of the voltage across it ($q = f(V)$). Then the i - v relation [19] could be written as

$$i = \frac{dq}{dt} = \frac{df}{dv} \frac{dv}{dt}$$

therefore,

$$\frac{dv}{dt} = \left(\frac{df}{dv} \right)^{-1} i.$$

Applying trapezoidal integration would yield

$$v(t + \Delta t) \approx v(t) + \frac{\Delta t}{2} \left(\left[\frac{df}{dv} \right]_t^{-1} i(t) + \left[\frac{df}{dv} \right]_{t+\Delta t}^{-1} i(t + \Delta t) \right) \quad (16)$$

where $\frac{df}{dv}$ is by definition the “capacitance”, therefore after a few modification and rearrangement, the relation for a non-

linear capacitor can be written as

$$v_c(t + \Delta t) - \frac{\Delta t}{2C(t + \Delta t)} i_c(t + \Delta t) = v_c(t) + \frac{\Delta t}{2C(t)} i_c(t). \quad (17)$$

At each time point, the capacitance value should be recalculated (based on component model and equations) and the rows in both A and b in MNA formulation has to be updated based on (17).

5 Numerical examples

To test the reliability of the developed solver, three examples involving a PEEC model with active circuit elements attached are given. The results are compared with the results from OrCAD [22] circuit solver. The PEEC model is of a transmission line (TL) and modeled as a 3D structure. The TL consists of two parallel, copper conductors ($l = 50$ mm, $w = 20$ μm , and $t = 1$ μm) separated by $d = 20$ μm . Each of the conductors are uniformly discretized with n_x , n_y , and n_z nodes along length, width, and thickness directions, respectively. By changing n_x , n_y , and n_z , size of the PEEC equivalent circuit changes and the number of resistors, capacitors, (partial) inductors, and mutual couplings changes accordingly. In Table 1 six different discretizations has been proposed. The number of resistors, self partial inductances, mutual partial inductances, self capacitors, and mutual capacitors in the equivalent circuit are represented for each discretization by R , L_p , K , C_{self} , and C_{mutual} respectively. In this section, it is assumed that $n_x = 20$, $n_y = 2$, and $n_z = 1$ (test case 3), which results in 204 volume cells and 126 surface cells. Hence the partial inductance matrix (L_p) is of the size 204×204 , and the coefficients of potential matrix (P) will be of the size 126×126 . In both examples, the developed solver is used to find the time domain response of the whole system including the transmission line and the lumped passive and active circuit elements connected to it. Then, a time domain simulation is done in OrCAD, using a 2D transmission line model (T-component), connected to

Fig. 4 BJT Ebers-Moll static model

Table 1 The number of circuit elements in the equivalent circuit for six different discretizations

Test case	$n_x \times n_y \times n_z$	R	L_p	K	C_{self}	C_{mutual}
1	$10 \times 2 \times 1$	104	104	2716	66	2123
2	$15 \times 2 \times 1$	154	154	6021	96	4528
3	$20 \times 2 \times 1$	204	204	10626	126	7833
4	$20 \times 3 \times 1$	286	286	20595	168	13944
5	$22 \times 3 \times 1$	314	314	24853	184	16744
6	$22 \times 5 \times 1$	494	494	61051	276	37766

Fig. 5 The bridge rectifier circuit

Fig. 6 Comparing PEEC and OrCAD results for rectifier in Fig. 5

the same lumped passive and active circuit elements (it has been shown in [23] that the OrCAD transmission line model used here has the same response).

5.1 Full-wave rectifier with PEEC model for transmission line

In the first example, a full-wave bridge rectifier circuit is connected to the transmission line, and a resistor is connected at the far end as the load. The schematic of the OrCAD circuit along with the values of all the components can be seen in Fig. 5. Voltage at the near end and far end of the transmission line, acquired from both OrCAD and the developed solver, are presented in Fig. 6. A good agreement between the results has been obtained.

5.2 BJT circuit with PEEC model for transmission line

The second example comprises of a BJT in which the collector output is connected to the transmission line and a load. The schematic is presented in Fig. 7. Studying the base-collector voltage and base-emitter voltage shows that the

BJT is operating as a common-emitter switch. Time domain response for the time period of 6 ns for PEEC and OrCAD are depicted in Fig. 8. DC values of selected set of node voltages and component currents are presented in Table 2. The results are in good agreement, and small deviations seen between the curves can be addressed to the different models used for the transmission line. OrCAD utilizes analytical models for transmission lines. Simulations of the same circuit without the transmission line shows a perfect match between the results from OrCAD and the developed solver, reflecting the fact that the developed solver and the component modelings are consistent with OrCAD.

5.3 Multi-stage amplifier

The third example is a four-stage bipolar amplifier shown in Fig. 9 [24]. The transistors Q_1 and Q_2 form the first differential-in, differential out stage, while Q_4 and Q_5 is a differential-in, single ended out stage. Shifting the dc level is achieved via Q_7 , and finally the output stage which is an emitter follower transistor Q_8 . Time domain response for PEEC and OrCAD at both ends of the TL are depicted in Fig. 10. The results are in good agreement, and again, deviations are originated from the different models used for the transmission line.

It is worth to mention that OrCAD utilizes the Gummel-Poon model [20] as the default BJT model. Gummel-Poon model is a more advanced and complex model for BJT in comparison to simple Ebers-Moll model, in which many of important second-order effects present in actual components are not included. Since the developed solver employs the Ebers-Moll model to simulate BJT, the BJT model in OrCAD is simplified by removing some of the parameters in the model definition. This model modification forces OrCAD to use Ebers-Moll model instead of Gummel-Poon model.

Fig. 7 The bipolar junction transistor in switching mode **Fig. 8** Comparing PEEC and OrCAD results for BJT working as a switch in Fig. 7

6 Feasibility analysis

In order to study the feasibility of the dedicated PEEC solver, two examples comprising a PEEC model are used. In the first example, studied in Sect. 6.1, only linear components are used. A sinusoidal voltage source is connected to one end of the TL, and the other end of the TL is terminated with a $50\ \Omega$ resistor. In the second example, examined in Sect. 6.2, the multi-stage amplifier circuit (nonlinear circuit) from Sect. 5.3 is studied. The dedicated PEEC solver solution time and SPICE solution time for different test cases (presented in Table 1) are measured and effective factors in the solution times are discussed.

6.1 Linear components

In this section, two linear components, a sinusoidal voltage source at one end and a $50\ \Omega$ resistor at the other end, are connected to different ends of a parallel plate transmission line. SPICE and the dedicated PEEC solver solution

Table 2 DC values of selected node voltages and branch currents for the circuit in Fig. 7

	SPICE	PEEC
$I(RC)$	$+5.83704 \times 10^{-12}$	$+5.83744 \times 10^{-12}$
$I(RE)$	$+5.01434 \times 10^{-12}$	$+5.01434 \times 10^{-12}$
$I(RS)$	-8.23102×10^{-13}	-8.23102×10^{-13}
$V(Q1B)$	$+4.11551 \times 10^{-11}$	$+4.19502 \times 10^{-11}$
$V(Q1E)$	$+4.26218 \times 10^{-10}$	$+4.36783 \times 10^{-10}$
$V(Q1C)$	$+5.0$	$+5.0$

times for six test cases (introduced in Table 1) are plotted in Fig. 11. By looking at *linear* curves, it can be seen that as the size of the PEEC model increases, the SPICE solution time increases drastically, while the PEEC solver solves the circuit in a more reasonable time (*non-linear* curves will be discussed in Sect. 6.2). To find out the reason behind this phenomenon, the MNA matrices and their structure for PEEC and SPICE are studied. As described in Sects. 3.1 and 3.2, the system of equations can be written as $Ax = b$, where both A and b should be updated at each time step. In Fig. 12, MATLAB's *spy* plot for matrix A of the PEEC solver for the PEEC model, test case 1, has been plotted. The matrix consists of two parts. The upper part ($P.\#1$) represents KVLs for RL branches, including a resistor, an inductor, and all the mutual couplings between the inductor and all other inductors in the circuit. The lower part ($P.\#2$) represents KCLs at all PEEC nodes (not the nodes between R and L in RL branches). It can be seen that the matrix is dense. The two dense blocks in the upper part construct the L_p matrix. This shape is directly related to the 2-D mesh of the physical structure under examination [8]. The dense block in the lower part is P^{-1} (refer to (6)). It should be noted that in any 2-D modeling, this structure will be seen in the MNA formulation since both L_p and P^{-1} matrices are full.

Fig. 9 The multi-stage amplifier circuit

Fig. 10 Comparing PEEC and OrCAD results for multi-stage amplifier depicted in Fig. 9

In Fig. 13 the *spy* plot for the same structure is plotted while the SPICE-MNA formulation has been used. First to notice is size increase of the matrix. While matrix size for the PEEC formulation is 171×171 , the SPICE-MNA formulation matrix has a size of 274×274 . For a PEEC model comprising N nodes (PEEC nodes) and M inductive (RL) branches, the MNA matrix in PEEC is $(M + N) \times (M + N)$ consisting of N KCLs at the PEEC nodes and M KVLs for

Fig. 11 Solution time for PEEC solver vs. SPICE

the RL branches. The MNA matrix for the same structure in SPICE will have N KCLs at PEEC nodes, M KCLs at *internal nodes* (new defined nodes between each resistor and inductor in the RL branches), and M KVLs for the self and mutual inductors. In other words, SPICE-MNA formulation has M unknowns more than that of PEEC-MNA. On the other hand, the sparsity (the number of non-zero elements to the size of the matrix) for SPICE formulation is around 14 %, while it is 35 % for the PEEC formulation. The top most part ($P.\#1$) represent KVLs for the inductors in the circuit. Two small dense block at the right of this section

Fig. 12 Spy plot for the PEEC-MNA formulation for test case 1

accounts for the mutual inductive couplings. The 2nd part (*P.#2*) includes KCLs for PEEC nodes where the dense part at the left is caused by self and mutual capacitors. The lower part (*P.#3*) represents KCLs at internal nodes.

The SPICE longer solution time could be caused by the mutual inductances, or the mutual capacitances. Both construct dense blocks in the formulation, that might slow down the sparse solver used in SPICE. To test this, first, all the mutual couplings (*K* components) are excluded from the circuit, which translates to having no mutual magnetic coupling between the volume cells. The solution time reduces to 7 seconds, compared to 25 seconds for the original structure, which is even faster than the PEEC solver for the whole structure. To eliminate this dense block and sparsify the SPICE-MNA formulation, other types of circuit components could be used instead of coupling coefficients (*K* component). One approach could be to replace the mutual couplings with dependent voltage sources. Two dependent voltage source V_{ij} and V_{ji} are added in series with inductors L_{ii} and L_{jj} , respectively, to account for the coupling between L_{ii} and L_{jj} . The voltage of each voltage source is related to the derivative of the current in the other inductor. For example, in Fig. 2, a voltage source $V_{12} = L_{12} \frac{dI_2}{dt}$ and another voltage source $V_{21} = L_{12} \frac{dI_1}{dt}$ should be added in series with L_{11} and L_{22} respectively ($K = L_{12}/\sqrt{L_{11}L_{22}}$). In this scenario two dependent voltage sources are appended to the circuit to account for each mutual magnetic coupling, which will cause the size of the MNA matrix to increase. In addition to matrix size increase, this type of dependent voltage source, where the voltage is dependent on the *derivative* of the current, is not supported in SPICE, and could be implemented only by modifying the SPICE source code.

In another test, all the capacitors are excluded from the circuit. This means that electric couplings inside the physi-

Fig. 13 Spy plot for the SPICE-MNA formulation for test case 1

cal structure are negligible, which actually might happen in power electronic systems where the frequency of operation is very low [25]. Surprisingly, the simulation time increases to 27 seconds which is more than the simulation time of the whole structure while capacitive terms are present. Simulations for other test cases show the same result. Eliminating the capacitive terms translates to removing the dense part of the second part (section *P.#2*) in Fig. 13. It is speculated that by sparsifying this system of equation, the SPICE sparse solver takes more time to converge or SPICE changes the algorithm for simulation, but since not much information is available about the internal mechanisms and algorithms used in the SPICE engine, it is impossible to reach a exact conclusion in this situation.

The last factor in the solution time is the effect of the size of the equivalent circuit. As the discretization becomes denser by increasing n_x , n_y , and n_z , the number of components in the equivalent circuit increases and SPICE requires more time to read the input file and build the net list for the circuit. As an example, SPICE spends about 10 minutes to build the net list for the test case 6 on a dual core 2.80 GHz CPU.

To conclude, the mutual magnetic couplings slow down SPICE iterative solver by building a dense block in the MNA formulation. Sparsifying the formulation, though impossible with the current version of SPICE, creates a huge system which might itself increase the solution time. It can be said that PEEC models are not suitable to be solved in SPICE, and SPICE solver fails to solve these type of systems of equations in a reasonable time and as the PEEC model increases in size, the SPICE solution time increases more drastically than that of the dedicated PEEC solver. Moreover, though not covered in this paper, SPICE, in its original form, can not be used in full-wave simulations where

the retardation effects can not be neglected (Full-wave simulation using SPICE is done in [10] by modifying an open source version of SPICE). A specialized solver can solve the PEEC systems in a much faster way, and also delays and retardation can be implemented in the solver [12]. On the other hand, as stated before, all the definitions and models of circuit devices e.g. transistors, MOSFETs, etc. should be implemented in this specialized solver. This implementation means programming and developing a new circuit solver inside the PEEC solver in order to read a component and construct the system of equations for that component, which is definitely not an easy task for complex components/devices.

6.2 Non-linear components

In this section effects of non-linear components on solution time are studied. For this purpose, the multi-stage amplifier circuit from Sect. 5.1 is used. SPICE and the dedicated PEEC solver solution time for six test cases (refer to Table 1) are plotted in Fig. 11 as *non-linear*. Here again, it can be seen that the solution time is noticeably smaller for the PEEC solver compared to SPICE. Also it is noticed that the PEEC-solver solution times are around 4 times larger than those of the same structure but without non-linear components. As discussed in Sect. 4.2, non-linear components are defined by their I – V relationships which change in response to the operating point of the component. Since the system equations represent linear relationships, these non-linear equations should be modified and *linearized* in order to be put in the MNA matrix formulation. *linearized* form of non-linear equations can be obtained by using the Taylor's expansion around a arbitrary value of $V = V_0$ as

$$I = G_{eq}V + I_{eq}, \quad (18)$$

in which G_{eq} and I_{eq} are functions of V_0 . This linearized form can be used in the MNA formulation. However, unlike the case of linear components, where potentials and currents at each time point are calculated in a single step, the Newton-Raphson algorithm [18] should be used at each time point for non-linear components. The Newton-Raphson algorithm updates the values of G_{eq} and I_{eq} at each iteration, (18) will be updated in the MNA formulation, the system $Ax = b$ will be solved until the solutions, x , between two successive iterations converge [18]. In normal situations, between 3–5 iterations are needed for the solution to converge at each time point, which implies that the system of equations $Ax = b$ should be solved 3–5 time more at each time point compared to the case where there is no non-linear components in the circuit. By defining α as

$$\alpha = \frac{t_{\text{nonlinear}}}{t_{\text{linear}}} \quad (19)$$

it can be seen in Fig. 11, by comparing the solution time of the PEEC solver in the linear and non-linear case, that $\alpha \approx 4$.

It is also interesting to notice that for the SPICE solution times $\alpha \approx 1.1$ where it is expected otherwise. This can be addressed to the *intelligent* iterative solver used in SPICE. When non-linear components exist in the circuit, only a few number of rows of matrices A and b changes between the iterations. In the developed PEEC solver, LU factorization is used at every iteration regardless of this fact. At each iteration the whole system is factorized and solved while the most part of the calculations are identical between two successive iterations. Apparently SPICE utilizes the matrix similarities and only does the necessary calculations. Using better factorization methods in the dedicated PEEC solver can avoid the redundant calculations and speed up the PEEC solver even more. At the end, it also should be noted that the discussion about α is a more qualitative discussion and the number of iterations in the Newton-Raphson algorithm can change depending on the circuit, the circuit activity, and the time step [18].

7 Conclusion

The implementation of active/non-linear circuit elements in the PEEC method for the aim of co-design of EM/circuit problems has been investigated. A specialized solver has been developed, where the Newton-Raphson algorithm has been used to solve the linearized system of equations. Three numerical tests including a transmission line have been presented to show the results. The results have been compared with OrCAD circuit simulation, where an analytical transmission line model is used. Good agreement between the results are observed. Feasibility of the specialized PEEC-solver is compared with the SPICE-solver in order to develop the optimal electromagnetic solver with the capability to simulate passive/active lumped circuit elements. The MNA formulation for PEEC models in both the specialized PEEC-solver and SPICE are extracted for a simple example. The size, sparsity and the pattern of the matrices, along with the solution time of the PEEC-solver and SPICE are compared. While SPICE is a powerful and readily available circuit solver, it takes quite long time to simulate PEEC structures compared to the dedicated PEEC solver. On the other hand, the PEEC-solver has a major issue which is all the passive/active circuit component models should be re-implemented in it, and a trade-off exists between the solution time and the implementation time. Implementing other component models e.g. MOSFETs in the dedicated solver or to find a hybrid method to integrate the dedicated solver and SPICE seem to be more reasonable options.

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