DC Generation for Inductively Coupled RFID Systems

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Abstract

The ability to store information electronically in small tags that can be read wirelessly has great potential. Radio frequency identification (RFID) technology is used today in a number of different areas, such as logistics, supply chain management, access control and environmental monitoring. Recently, research on RFID technology has focused on sensor tags, localization techniques, antennas and propagation, data security, communication protocols and circuit design for the tags and the readers.

In a typical RFID system, a passive tag is powered up remotely by a radio frequency signal sent from a reader unit. The RF signal received by the tag antenna is converted to a DC-supply voltage by the rectifier in the analog front-end of the tag. To avoid power loss in the rectifying operation, low-voltage Schottky diodes are often used in a multi-stage rectifier. However, the use of Schottky diodes is not cost efficient because these diodes must be designed in advanced semiconductor processes. Because one of the demands on future RFID technology is to reduce the cost, efficient rectifiers that can be integrated in a low cost semiconductor process is highly desirable. For this reason, different rectifiers in standard CMOS have been proposed.

This thesis discuss recent work and present new ideas on rectifiers in CMOS that have the potential to replace Schottky diodes in rectifiers for low-power RFID applications. The design and modelling of multi-stage rectifiers for maximized DC generation in an inductive RFID system are also included. Furthermore this thesis presents techniques for inductive transponders that allow improved DC generation and reduced orientation sensitivity for transponders that trace moving objects.

Part I of the thesis presents a theoretical analysis of the RF to DC generation using single diode rectifiers. This analysis illustrates how different properties, such as the voltage and power conversion efficiency of the rectifier, the Q-factor of the resonance circuit and the coupling coefficient between coil antennas, affect the tag DC generation. Furthermore, Part I also discusses DC generation for inductive transponders using multiple coil antennas. In Part II, Paper A discusses the limitations with the CMOS cross-connected bridge rectifier and proposes a modified bridge with active diodes to improve rectifier performance. Paper B presents a theoretical model for diode-connected MOS transistors with internal threshold cancellation (ITC), as well as a design procedure that describes how to optimize a rectifier based on MOS ITC diodes. In Paper C a highly efficient active MOS diode is presented that can be used in multi-stage low-power rectifiers. In addition, this study shows that active diodes in CMOS can be designed to have a diode voltage drop of less than 100 mV and have a power consumption of a few μW. Paper D presents a model for the DC charge-up phase in a rectifier driven by a coil antenna. This model
was used to determine the available chip current in a typical pulsed RFID system. In Paper E, the modeling and design of multi-stage rectifiers for inductively coupled RFID tags is presented. Finally, Paper F presents front-end circuit solutions for transponders using multiple coil antennas.

The work presented in this thesis demonstrates that highly efficient RF to DC conversion can be achieved using CMOS rectifiers for low-power applications. New techniques in CMOS with the potential to replace Schottky diodes in RFID rectifiers are demonstrated. Furthermore, new design criteria for voltage multipliers to achieve maximized DC generation in inductively coupled RFID tags and techniques for reduced orientation sensitivity are presented. These results are promising for improving and reducing cost of inductively coupled RFID systems.
CONTENTS

Part I 1

CHAPTER 1 - THESIS INTRODUCTION 3
  1.1 Objective ................................... 4
  1.2 Outline ..................................... 4

CHAPTER 2 - RFID TECHNOLOGY 5
  2.1 Historical Background ............................ 5
  2.2 Principles of Operation ............................ 6
  2.3 Standards and Properties ........................... 8
  2.4 Typical Tag Architectures .......................... 9

CHAPTER 3 - TAG DC GENERATION 13
  3.1 The DC Generation System ......................... 13
  3.2 Recent Research in CMOS Rectifier Design .......... 20

CHAPTER 4 - MULTIPLE COIL ANTENNA DC GENERATION 27
  4.1 Cascaded DC Generation ........................... 27
  4.2 Front-end Architecture ............................ 31

CHAPTER 5 - SUMMARY OF THE PAPERS 33
  5.1 Paper A .................................... 33
  5.2 Paper B .................................... 33
  5.3 Paper C .................................... 34
  5.4 Paper D .................................... 34
  5.5 Paper E .................................... 34
  5.6 Paper F .................................... 35

CHAPTER 6 - THESIS SUMMARY 37
  6.1 Conclusion ................................... 37
  6.2 Future Work .................................. 38

REFERENCES 39

Part II 43

PAPER A 45
  1 Introduction ..................................... 47
<table>
<thead>
<tr>
<th>Paper</th>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>Introduction</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>Internal Threshold Cancellation</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td>Bridge Rectifier with ITC</td>
<td>62</td>
</tr>
<tr>
<td></td>
<td>Results</td>
<td>66</td>
</tr>
<tr>
<td></td>
<td>Conclusion</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td>Acknowledgements</td>
<td>71</td>
</tr>
<tr>
<td>C</td>
<td>Introduction</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td>Threshold Cancellation</td>
<td>77</td>
</tr>
<tr>
<td></td>
<td>Proposed Diode</td>
<td>79</td>
</tr>
<tr>
<td></td>
<td>Results</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>Conclusion</td>
<td>82</td>
</tr>
<tr>
<td></td>
<td>Acknowledgements</td>
<td>84</td>
</tr>
<tr>
<td>D</td>
<td>Introduction</td>
<td>87</td>
</tr>
<tr>
<td></td>
<td>Model</td>
<td>89</td>
</tr>
<tr>
<td></td>
<td>Results</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td>Conclusion</td>
<td>94</td>
</tr>
<tr>
<td></td>
<td>Acknowledgements</td>
<td>98</td>
</tr>
<tr>
<td>E</td>
<td>Introduction</td>
<td>101</td>
</tr>
<tr>
<td></td>
<td>Modelling The N-stage Voltage Multiplier</td>
<td>103</td>
</tr>
<tr>
<td></td>
<td>The Active Diode in CMOS</td>
<td>105</td>
</tr>
<tr>
<td></td>
<td>Proposed CMOS Voltage Multiplier</td>
<td>112</td>
</tr>
<tr>
<td></td>
<td>Measurement Results</td>
<td>116</td>
</tr>
<tr>
<td></td>
<td>Conclusion</td>
<td>119</td>
</tr>
<tr>
<td></td>
<td>Acknowledgements</td>
<td>124</td>
</tr>
<tr>
<td>F</td>
<td>Introduction</td>
<td>127</td>
</tr>
<tr>
<td></td>
<td>Select</td>
<td>129</td>
</tr>
<tr>
<td></td>
<td>FSK modulation front-end</td>
<td>131</td>
</tr>
<tr>
<td></td>
<td>Cascaded DC generation</td>
<td>132</td>
</tr>
<tr>
<td></td>
<td>Measurement results</td>
<td>139</td>
</tr>
<tr>
<td></td>
<td>Conclusion</td>
<td>142</td>
</tr>
<tr>
<td></td>
<td>Acknowledgements</td>
<td>147</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>--------------------------------------</td>
<td></td>
</tr>
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<td>AC</td>
<td>Alternative Current</td>
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<td>Austria Micro Systems</td>
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<td>ASK</td>
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<td>Binary Frequency Shift Keying</td>
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<td>Binary Phase Shift Keying</td>
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<td>BW</td>
<td>Bandwidth</td>
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<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
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<td>DC</td>
<td>Direct Current</td>
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<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
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<td>EM</td>
<td>Electro Magnetic</td>
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<td>EOB</td>
<td>End Of Burst</td>
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<td>EPC</td>
<td>Electronic Product Code</td>
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<td>EVC</td>
<td>External Threshold Cancellation</td>
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<td>Frequency Shift Keying</td>
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<td>FTC</td>
<td>Full Threshold Cancellation</td>
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<td>GHz</td>
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<td>HDX</td>
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<td>HF</td>
<td>High Frequency</td>
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<td>IC</td>
<td>Integrated Circuit</td>
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<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
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<td>ISO</td>
<td>International Organization for Standardization</td>
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<tr>
<td>ITC</td>
<td>Internal Threshold Cancellation</td>
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<td>Internal Threshold Cancellation</td>
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<td>LF</td>
<td>Low Frequency</td>
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<td>MHz</td>
<td>Mega Hertz</td>
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<td>MOS</td>
<td>Metal Oxide Semiconductor</td>
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<td>NFC</td>
<td>Near Field Communication</td>
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<td>PCE</td>
<td>Power Conversion Efficiency</td>
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<td>Sequential Systems</td>
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<td>SMA</td>
<td>Surface Mount Assembly</td>
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<td>SNR</td>
<td>Signal to Noise Ratio</td>
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<td>SOI</td>
<td>Silicon On Insulator</td>
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<td>Silicon On Sapphire</td>
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<td>Ultra High Frequency</td>
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<td>VCE</td>
<td>Voltage Conversion Efficiency</td>
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Hans Rabén
Part I
Since the first commercial applications of radio frequency identification (RFID) in the late 1960s, the development of RFID has continued to expand into new markets, and new application areas have been discovered. The vision of RFID as a technology with the same potential as the internet to affect our daily lives and the potential to impact every business sector has been widely discussed. However, despite positive market predictions for the expected world wide adoption of RFID technology, the development of this technology is still working to cross the chasm between the early market and the mainstream market [1].

There are several reasons why the global adoption of RFID technology has not been as fast as predicted. The main reason is the relatively high cost of RFID tags, which include the costs of the IC chip, the antenna and the tag assembly [2,3]. Efforts to lower the cost include the use of low-cost semiconductor technologies in the chip design and the development of less expensive assembly processes. This development is also favored by the rapid drop in the price of IC chips. In 2006, SmartCode Corp. announced a cost of 5 cents per tag in quantities of 100 million, which was considered to be a milestone. Regarding the application of ultra-low-cost tags (< 1 cent) as bar code replacements, current research on RFID also includes tags in printed electronics using polymer-based semiconductor technologies and microstrip-based chipless RFID [4,5].

In addition to the cost, the second hurdle in the adoption of RFID systems is reliable reading. The reliability is affected by several factors that cause variations in the received signal strength in the tag and the reader antenna. One important factor is the orientation of the antennas, which results in large variations in the reliable reading range. Performance degradations also occur because of the materials on which the tag is attached. Advanced antenna techniques along with reduced chip power consumption can improve the reliable reading range [6], and the use of magnetically coupled RFID can limit degradation due to lossy materials in the environment [7].

The final difficulty that has placed future demands on RFID technology is data security and privacy. The conventional approach to securing RFID communication is encrypting the tag ID [8]. However, the security is often compromised because the limited available chip power prohibits the implementation of full-strength encryption keys.
1.1 Objective

A passive tag receives its power remotely from the energy in the radio signal that is transmitted from the reader antenna. The signal levels received by the tag antenna can be very small, which makes it difficult to rectify and utilize the energy in an initially powerless tag. The overall aim of this thesis is to find circuit solutions that efficiently utilize the tag energy in the RF to DC conversion. Considering the abovementioned future demands on RFID technology, the following research questions have been identified for this thesis:

- **Q1**: Can rectifiers in CMOS be made more efficient to improve the power budget of a chip to allow additional functionality?
- **Q2**: Can rectifiers in CMOS replace rectifiers based on Schottky diodes that are used in advanced semiconductor processes?
- **Q3**: Can multiple coil antennas be used in inductive transponders for improved DC generation and reduced orientation sensitivity?

1.2 Outline

This thesis is organized as follows. Chapter 2 provides a brief introduction to RFID technology to outline the basic concepts of RFID that are described in the literature. In Chapter 3, a detailed analysis is presented of the DC generation system for magnetically coupled RFID. A theoretical model is developed to investigate how different parameters affect the conversion. This chapter also includes a review of recent work in CMOS rectifiers. In Chapter 4, DC generation using multiple coil antennas is further studied based on Paper F. Additionally, the design and simulation results of a front-end architecture in CMOS for FSK modulation and cascaded DC generation are presented. A summary of the papers in this thesis is provided in Chapter 5, and the thesis is concluded in Chapter 6. The papers are reformatted and reprinted in Part II.
2.1 Historical Background

The history of RFID communication dates back to the early 20th century with the discovery of radar technology. Many communication applications based on back-scattered radio waves were developed from which passive RFID technology originates [3]. As a brief historical background, a chronology starting with this development is presented below.

- 1940: During World War II the British developed a transponder that relied on passive radar reflectors for the Identify Friend-or-Foe system (IFF).
- 1945: Leon Theremin used a passive technique to transmit audio signals, which is considered to be a predecessor of RFID technology.
- 1948: The RFID-related paper "Communication by Means of Reflected Power" is published [9].
- 1963: A passive RFID transponder using EM coupling and energy rectification was patented by Richardson.
- 1960s: The first commercial application of RFID was introduced: Electronic Article Surveillance (EAS).
- 1975: The concept of tag antenna load modulation was introduced at Los Alamos Scientific Laboratory.
- 1980s: RFID was used in transportation, personnel access, animal tracking and electronic toll collection applications.
- 1990s: RFID global standards (ISO) for animal tracking and proximity cards were developed.
RFID Technology

Figure 2.1: Near-field communication using inductive coupling [3]. Copyright © 2007 IEEE. Figure reprinted with permission.

- 1995: The first integrated circuit RFID tags were developed [10].
- 2002: The Near-Field Communication Forum (NFC) introduced mobile phones equipped with RFID readers.
- 2003: Integrated UHF RFID was introduced [11].
- 2005: Wal-Mart (USA) began implementing EPC RFID for item tagging.

2.2 Principles of Operation

2.2.1 Near-Field and Far-Field Coupling

There are two types of coupling techniques that are used between the reader and the tag in RFID technology: near-field coupling and far-field coupling.

In the near-field region, the coupling between the reader and the tag depends on the magnetic field through inductive coupling using coil antennas, as illustrated in Fig. 2.1. The communication from the tag to the reader occurs through a mechanism called load modulation, where a continuous RF signal that is sent from the reader is modulated in

\footnote{Although less common, the near-field system can also employ capacitive coupling through the electric field between reader and tag.}
2.2. Principles of Operation

the tag by loading the tag coil in beat with a data signal \[7\]. As a result the modulated signal can be detected in the reader antenna through the transformer coupling between the two antennas. Load modulation of the continuous RF signal received by the tag coil is achieved by switching either a resistive load or a capacitive load in parallel with the resonance circuit. A capacitive load modulator is often chosen to avoid that poor RF isolation in the modulator in combination with a resistive load create unwanted loading effects, as further described in \[12\]. In addition to load modulation, the communication to the reader can also be achieved by transmission from the tag, where a local oscillator is used to generate the carrier. Both communication techniques are further discussed in Section 2.4.

In the far-field region, the magnetic coupling between the antennas is lost and the emitted field has developed into a freely propagating EM wave \[7\]. The separation of the EM wave from the emitting antenna begins at the distance \(d = \lambda/2\pi\), where \(\lambda\) is the wavelength of the emitted wave. Consequently, radio antennas are used for communication in the far-field region. The modulation technique used is called backscattering and is achieved by varying the mismatch between the tag antenna and its loading circuit such that the amount of energy reflected to the reader antenna is varied.

2.2.2 Duplex Techniques

A brief introduction to the different methods for transferring power to a tag, along with the read and write procedure between the reader and the tag, is presented below:

- **Half Duplex (HDX)**
  In the half-duplex procedure, the data transfer alternates between downlink and uplink communication, as shown in Fig. 2.2. The methods used are load modulation and backscatter modulation. Both methods are based on simple circuitry.

- **Full Duplex (FDX)**
  In the full-duplex system, the data transfer is performed simultaneously using down-
link and uplink communication. In this communication system, the reader and the tag transmit at different carrier frequencies, allowing the tags to be read at a higher rate. Full duplex tags are currently used in both inductive and radiative systems [13].

- **Pulsed System (SEQ)**
  In the pulsed system, which is also termed the sequential system, the energy transfer to the tag alternates with uplink data transfer. This procedure, in which the uplink transmission is achieved by the use of a local oscillator, allows for a longer reading range while the tags are read at a lower rate.

### 2.3 Standards and Properties

Several standards have been developed by ISO to specify the air interface, code and command structure and the applications in RFID communication. The two most common standards are ISO 11784 (125 kHz) for animal identification and ISO 14443 (13.56 MHz) for proximity cards [14]. The standard for UHF (915 MHz) is EPCglobal, which was developed for product labeling by Auto-ID labs [15]. A comparison of the characteristics for different RFID frequencies and their corresponding standards are shown in Fig. 2.3. Additional comments on the frequency characteristics of the RFID system in Fig. 2.3 are summarized below:

- **Reading Range**
  Long reading range systems are typically based on UHF RFID because the free-space path loss is significantly lower for radiative than for inductive RFID.

- **Data Rate**
  A high carrier frequency allows for higher data rates because of the larger available
2.4 Typical Tag Architectures

Integrated circuit passive RFID tags were introduced for low-frequency (LF) [10] and ultra-high-frequency (UHF) [11] RFID applications in 1995 and 2003 respectively. Two different inductive tags are discussed below: One read-only LF tag for the pulsed system and one read-write HF tag. The architecture of an UHF tag is also briefly commented.

Read-only LF tag

Fig. 2.4 shows the block diagram of a typical tag for the pulsed system (SEQ) operating in the LF band. The tag is a read-only device which means that the tag ID can be read by uplink data transfer, while downlink data transfer is not allowed. A read-write device for the pulsed system can, in addition to transferring data uplink, also receive instructions and be programmed by downlink data transfer [16]. The read-only tag for the pulsed system operates in two phases: one charge-up phase where the reader sends an RF burst to power up the tag, followed by a transmission phase when the tag sends data to the reader, as further described in Paper D, Paper F and in [10, 17, 18]. The functional blocks of the tag is briefly described below.

Figure 2.4: Functional block diagram of a tag for the pulsed RFID system (SEQ) operating in the low frequency band. The figure is based on [7].
The resonance circuit: The resonance circuit is tuned at the RF frequency (125 kHz) that is transmitted from the reader to power up the tag. A voltage step-up of the weak, induced signal in the coil is achieved so that the amplitude exceeds the minimum turn-on voltage of the rectifier.

The rectifier block: AC to DC conversion is performed in the rectifier block to generate the supply voltage $V_{dd}$ that supplies all active circuit blocks on the chip during the transmission phase of the tag.

The EOB detector: To end the charge-up phase, the reader signal is turned off. An end-of-burst signal is generated by the EOB circuit block that activates all the circuits required for uplink transmission, which have been in power down mode during charging.

Binary FSK modulation: When the oscillator is activated, a carrier for uplink transmission is generated in the resonance circuit, which is used as the frequency determining component in the oscillator. A data signal is generated by the shift register of the tag which is connected to the EEPROM memory where the tag ID is stored. The data is then sent by means of binary FSK modulation (BFSK) which is achieved by switching a capacitor in parallel with the resonance circuit in beat with the data signal.

Clock generation: The clock that is required for the digital circuit blocks is generated by dividing the carrier to the desired clock frequency for data transmission.

Discharge: The transmission phase is ended by discharging the storage capacitor to ensure a safe Power-on-Reset at the next charge-up phase of the transponder.

Read-write HF tag

To indicate the main differences between the tag architecture above, that use the SEQ procedure, and that of a tag using the HDX procedure (Fig. 2.2), the functional blocks of the HF tag shown in Fig. 2.5, is briefly discussed below.

Rectifier: The DC supply is generated by the continuous RF signal that is sent from the reader so that the tag is supplied with stable DC during both the downlink and the uplink transmission.

Demodulator: The data transfer from the reader to the tag is achieved using 10 % ASK modulation of the RF carrier. The envelope of the modulated carrier is detected by the rectifier block. Thus, the rectifier both generates the DC supply and operates as envelope detector$^2$. ASK demodulation is performed in the demodulator block, which is connected to the output of the rectifier. The small changes of the RF envelope in combination with chip process and temperature variations as well as a large dynamic range of the input signal makes the demodulator block a challenge in the design of a HF tag [19].

Load modulator: Uplink data transfer is achieved by means of capacitive load modulation of the continuous RF signal that is sent from the reader. Here load modulation

$^2$Note the similarity between a rectifier and the AM detector which is used to demodulate an amplitude modulated signal.
2.4. **Typical Tag Architectures**

![Functional block diagram of the analog front-end of a HDX tag operating in the HF band](image)

*Figure 2.5: Functional block diagram of the analog front-end of a HDX tag operating in the HF band [19]. The tag is fully integrated in 0.18 µm process with a CoSi$_2$ Schottky diode and EEPROM process. Copyright © 2011 IEEE. Figure reprinted with permission.*

with subcarrier is used: Instead of driving the load modulator directly with the data signal of the tag, the modulator is driven by a subcarrier that has been modulated by the data. The subcarrier is modulated using binary phase shift keying (BPSK). Load modulation with subcarrier is used to simplify the detection of the received data in the reader compared to conventional load modulation [7].

**Regulator:** The tag uses two separately regulated supply voltages; one for analog circuits and one for digital circuits. This is to avoid that voltage ripple and digital switching noise affect the operation of the sensitive analog circuits, including the ASK demodulator.

**Clock extractor:** The clock signal for the chip is extracted from the incoming RF signal in the input resonance circuit before it is divided to the required clock frequency.

**UHF tag**

The architecture of a tag for the UHF band, that use radio antennas instead of magnetically coupled coils, are commonly implemented in advanced semiconductor processes such as SOI and SOS, which allows for the use of a high quality matching network to power-match the radio antenna to the rectifier input [22]. An additional difference between the architecture of a typical UHF tag and an inductive tag, is that the clock of the UHF tag is often generated by an on-chip oscillator [20,21]. This allows for reduced power consumption compared to the use of frequency dividers to generate the clock from the carrier.
CHAPTER 3

Tag DC Generation

This chapter serves as an introduction to DC generation for passive RFID tags, and as a background for the studies presented in Paper A-E, which are related to research questions Q1 and Q2, stated in Chapter 1.

The first part of this chapter presents theoretical studies and discusses different properties of the tag DC generation system. The second part presents recent work on RFID rectifiers in CMOS.

3.1 The DC Generation System

In this section, the derivation of a theoretical model for a DC generation system using a single diode rectifier, is presented. This model is further developed in Paper E for multi-stage rectifiers. This section also presents a study that demonstrates how the rectifier efficiency can affect the distance between the reader and tag coils. Further studies are included that show how the distance between coils affects the signal-to-noise ratio in the reader during uplink transmission from the tag in a pulsed RFID system. Finally, the turn-on voltage of the rectifier is also discussed.

Figure 3.1: DC generation using transformer coupled coil antennas typical for RFID near-field communication.
3.1.1 Theoretical Model

The wirelessly powered system shown in Fig. 3.1 consists of two inductively coupled coil antennas $L_1$ and $L_2$. A field is transmitted from the reader to power up the passive tag ($R_L$). A resonance circuit ($L_1, R_1, C_1$) provides a voltage magnification of the weak signal $u_i$ induced in the tag coil antenna before AC to DC conversion is achieved in the rectifier block. A simplified theoretical model for this system is derived below to illustrate how the rectifier efficiency affects the DC generation. Based on Fig. 3.1, the following relations are given:

- The rectifier input power:

$$P_{IN} = \frac{\dot{V}_{IN}^2}{2R_{IN}}. \quad (3.1)$$

To simplify the model, the nonlinear rectifier input impedance is modeled with a time-constant input resistor $R_{IN}$ that is calculated from the mean input power $P_{IN}$ [22].

- The DC output power:

$$P_{dc} = \frac{V_{dc}^2}{R_L}. \quad (3.2)$$

- The voltage conversion efficiency:

$$\eta_v = \frac{V_{dc}}{\dot{V}_{IN}}. \quad (3.3)$$

- The power conversion efficiency:

$$\eta_p = \frac{P_{dc}}{P_{IN}}. \quad (3.4)$$

- The quality factor $Q$ of the resonance circuit [7] with the resistive load $R_{IN}$ at resonance:

$$Q = \frac{1}{\frac{R_0}{2\omega_L} + \frac{\omega L_2}{R_{IN}}}. \quad (3.5)$$

- The peak input voltage to the rectifier at resonance:

$$\dot{V}_{IN} = Q\dot{u}_i. \quad (3.6)$$
3.1. The DC Generation System

Based on equations (3.3), (3.5) and (3.6) the DC output voltage is given as

$$V_{dc} = \eta_v Q \hat{u}_i = \frac{\eta_v \hat{u}_i}{RL \omega L_1 + \frac{R_2 \omega L_1}{\eta_p R_L}}.$$  (3.7)

To eliminate the unknown input resistance, equations (3.1) - (3.4) are combined and solved for $R_{IN}$. Substituting the result into (3.7), the DC output voltage can be written as

$$V_{dc} = \frac{\hat{u}_i}{RL \omega L_1 + \frac{R_2 \omega L_1}{\eta_p R_L}}.$$  (3.8)

The maximum DC output voltage is generated when the rectifier is unloaded and the voltage conversion efficiency is at a maximum. Equation (3.8) then simplifies to

$$V_{dc} = \frac{\hat{u}_i \omega L_1}{RL} = \hat{u}_i Q_1.$$  (3.9)

where $Q_1$ is the quality factor of the tag coil antenna.

Equation (3.8) also indicate that there is a trade-off between the voltage and the power conversion efficiency in RFID rectifiers, and that a high power conversion efficiency becomes increasingly important for larger current loads. The trade-off between the voltage and the power conversion efficiency is shown in Paper C of this thesis.

To verify this model, a single MOS diode rectifier was simulated in Cadence with a resonance circuit on the input and the resistive load on the output, as shown in Fig. 3.1. The simulation was performed with a sinusoidal input signal $u_i$ at 125 kHz and with the component values of the resonance circuit shown in Table 3.1. The simulated efficiency for the rectifier and the verification of the model is shown in Fig. 3.2 (left) and (right) respectively. In the verification of the model (right), $V_{dc}$ is plotted based on (3.8) after introducing the simulated efficiency $\eta_v$ and $\eta_p$ as a function of the induced peak voltage.
A simulation of the output voltage $V_{dc}$ is plotted along with the theoretical model, and they show good agreement.

### 3.1.2 Rectifier efficiency and range

In many applications, the achievable range for power up and data transfer is of interest. One example of how the rectifier efficiency affects the DC conversion in terms of an increased maximum distance between the coil antennas is shown in Fig. 3.3. In this example, when both $\eta_p$ and $\eta_v$ are increased from 0.5 to 0.8, the induced voltage required to generate 1.5 V DC is reduced from 57 mV to 38 mV ($\Delta \hat{u}_i = 19$ mV) with a 50 kΩ load. According to Fig. 3.3 (right), in which $\hat{u}_i$ is plotted as a function of the distance between the coils, this reduction represents an increase in the reading range of ca. 15%.

The right-hand graph in Fig. 3.3 was plotted based on the equation for the induced peak voltage, which is given as

$$\hat{u}_i = \omega \hat{i}_2 k \sqrt{L_1 L_2},$$

(3.10)

where the term $k \sqrt{L_1 L_2}$ is the mutual inductance between the reader and the tag coil antennas (with parallel windings centered on the same axis) and $\hat{i}_2$ is the peak current in the reader coil [7]. The coupling coefficient $k$ for a distance $x$ between the coils is given as

$$k = \frac{r_1^2 r_2^2}{\sqrt{r_1 r_2} (\sqrt{x^2 + r_2^2})^3},$$

(3.11)

where $r_1$ and $r_2$ are the radii of the tag and reader coils respectively, with the component values presented in Table 3.1. The reader coil $r_2$ is from a typical handheld RFID reader in which the peak current $\hat{i}_2$ is 1 A. Expressed in dB, the coupling coefficient can be rewritten as

$$k_{db} = 30 \log(r_1 r_2) - 60 \log x \quad \text{for } x >> r_2.$$  

(3.12)

The rapid attenuation of the magnetic field originates from the rightmost term, which is 60 dB/decade. Thus, the induced voltage is reduced from 1 mV to 1 μV when the distance is increased from 1 dm to 1 m. The above equations indicate that the reading range is favored by increasing both the inductance and the radius of the reader coil. This is also illustrated in Fig. 3.3 (right), where the red trace is representative of a reader coil with an inductance of 1.5 mH and a radius of 30 cm. However, compared to the small reader coil, the power dissipation in the reader coil $P_2 = I_2^2 R_2$ will increase 10 times as the coil resistance $R_2 = \omega L_2 / Q_2$.

<table>
<thead>
<tr>
<th>$L_1$</th>
<th>$R_1$</th>
<th>$C_1$</th>
<th>$L_2$</th>
<th>$r_1$</th>
<th>$r_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>155 μH</td>
<td>2 Ω</td>
<td>10.5 nF</td>
<td>150 μH</td>
<td>0.5 cm</td>
<td>3 cm</td>
</tr>
</tbody>
</table>
3.1.3 Range and SNR

It is also of interest to investigate how the distance $x$ will affect the transmission uplink from the tag to the reader coil in Table 3.1 after the supply voltage $V_{dc}$ has been generated. In the calculation below, a pulsed LF system is assumed, in which the tag sends an FSK modulated response using a local oscillator supplied by $V_{dc}$, as described in Paper F. To simplify this calculation, it is assumed that $V_{dc}$ is generated using an ideal single diode and that the available charge-up time allows the storage capacitor $C_s$ to be fully charged (3.9). The DC charge-up phase of the rectifier is further discussed in Paper D in this thesis. Given the induced coil voltage $\hat{u}_i$ (Fig. 3.3 right), the generated supply voltage can be written as

$$V_{dc} = \hat{u}_i Q_1.$$  \hfill (3.13)

The peak current in the tag coil during transmission as a function of the distance $x$ then becomes

$$i_1 = \frac{\hat{v}}{X_{L_1} + R_1} = \frac{V_{dc}}{X_{L_1} + \frac{x_1}{Q_1}} = \frac{u_i Q_1}{X_{L_1}(1 + \frac{x_1}{Q_1})} \approx \frac{u_i Q_1}{X_{L_1}} \quad \text{for} \quad Q_1 \gg 1, \hfill (3.14)$$

where $\hat{v}$ and $X_{L_1}$ are the peak voltage in the FSK modulator and the reactance of the tag coil, respectively. Substituting (3.14) into (3.10) provides the induced signal voltage in the reader coil $u_i$ so that the signal-to-noise ratio $SNR$ can be calculated from

$$SNR = \frac{s_i}{e_{n_2}} = \frac{u_i}{\sqrt{4R_2k_BT}} = \frac{u_i \omega k \sqrt{L_1 L_2}}{R_1 \sqrt{4R_2k_BT}} \hfill (3.15)$$

where $k_b$ is the Boltzmann constant, $T$ is the absolute temperature, and $B$ is the required bandwidth for a binary FSK signal with the frequency deviation $\Delta f$ and the bit rate $1/T_b$. Here,
Figure 3.4: The transponder supply voltage and the SNR in the reader antenna versus the distance for a pulsed RFID system. The supply voltage is plotted based on (3.13) and the SNR is plotted based on (3.15) for an FSK signal with $\Delta f = 11$ kHz and bit rate $1/T_b = 8$ kb/s.

$$B = 2(\Delta f + \frac{1}{2T_b})$$

(3.16)

and $R_2$ is the resistance of the reader coil given by

$$R_2 = \frac{X_{L_2}}{Q_2} = \frac{wL_2Bf_0}{Q_2}$$

(3.17)

The tag supply voltage and the signal-to-noise ratio in the reader are plotted in Fig. 3.4. This plot shows that a $V_{dc}$ in the mV range is theoretically sufficient to achieve an acceptable SNR of 10 dB in the reader coil, which would result in a maximum range of ca 0.6 m for this example. This assumes perfectly aligned coils in an environment with only thermal noise present and without signal interference.

### 3.1.4 Rectifier turn-on voltage

Another parameter that is important in the DC generation system is the turn-on voltage of the rectifier [23]. The turn-on voltage $V_{to}$ is the minimum peak input voltage to the rectifier$^1$ that can generate a DC voltage from the output. From this definition the minimum voltage induced in the tag coil that can be rectified, can be derived as a measure of the tag sensitivity. Given the turn-on voltage, the minimum induced input voltage can be written as

$$\dot{u}_{in} = \frac{V_{to}}{Q}$$

(3.18)

$^1$For a rectifier in CMOS, the turn-on voltage is typically equal to the threshold voltage $V_{th}$ of a MOS transistor.
where $Q$ is the quality factor of the input resonance circuit given by (3.5). Combining (3.5) with (3.1) and (3.4), and substituting the result in (3.18) yields an expression for the tag sensitivity as

$$\hat{u}_{ic} = \frac{V_{to}R_1}{\omega L_1} + \frac{2P_{dco}\omega L_1}{\eta_{pe}}V_{to}$$

(3.19)

where $\eta_{pe}$ and $P_{dco}$ are the power conversion efficiency and the DC output power of the rectifier at the turn on voltage $V_{to}$, respectively. Equation (3.19) indicate that the sensitivity is favored by improved power conversion efficiency, and that the equation simplifies to

$$\hat{u}_{ic} = \frac{V_{to}}{Q_1}$$

(3.20)

when the rectifier is unloaded.

The DC output voltage that is generated by $\hat{u}_{ic}$ can be written, based on (3.3), as

$$V_{dco} = V_{to}\eta_{pe}$$

(3.21)

where $\eta_{pe}$ is the voltage conversion efficiency of the rectifier when it is driven by the peak input voltage $V_{to}$. Here $\eta_{pe}$ must be larger than one to generate a DC output voltage that is sufficiently large to supply a typical transponder chip. This is commonly achieved through the use of a voltage doubler (Fig. 3.10) or several rectifiers in a charge pump configuration, which is further discussed in Paper E.
3.2 Recent Research in CMOS Rectifier Design

Rectifiers for RFID tags often use low-voltage Schottky diodes to reduce loss in the RF to DC conversion [11, 24]. However, Schottky diodes in a semiconductor process have high manufacturing costs compared to rectifiers designed in standard CMOS and a large temperature dependence [25–27]. Different rectifiers in standard CMOS have been proposed for RFID applications in which minimizing the cost is an important goal [28–36].

In the following section, a brief review of proposed techniques in a CMOS-only implementation for RFID tags is presented. The described techniques are different solutions to reduce the voltage drop in a rectifier without using low-voltage drop transistors or Schottky diodes or other techniques that are available in advanced semiconductor processes. The reviewed work includes

- Two active diodes based on comparator-driven switches
- Three MOS diodes with threshold cancellation techniques

3.2.1 Active diodes

In [30], an active bridge rectifier in CMOS was proposed that could be employed in wirelessly powered biomedical implants and passive RFID tags. As shown in Fig. 3.5 (b) two of the diodes in the full-wave bridge 3.5 (a) have been replaced with one pair of cross-connected pMOS switches. Both switches are driven by the full input swing and turn on as the peak input voltage exceeds the threshold voltage for each transistor switch. With sufficiently large transistor widths, such that $R_{on}$ is minimized, the voltage drop on each switch will be negligible.

To further reduce the peak loss in this bridge, both of the bottom diodes are replaced with a pair of active diodes with reverse current control as shown in Fig. 3.5 (c). Each diode is realized with an nMOS switch, which is driven by a 4-input comparator to achieve the desired high-speed switching action. The comparators are designed to be self-powered and biased by the input signal because there is no DC voltage supply in the system before
3.2. Recent Research in CMOS Rectifier Design

an input signal is applied. The advantage associated with the reduced voltage drop is not only to generate an increased voltage conversion efficiency, but also to reduce the power dissipation due to the forward current in the channel of each transistor. The simulated power and voltage conversion efficiency with a load resistor of 1.8 kΩ is shown in Fig. 3.6. The characteristics of the efficiency indicate that because of the complex active diodes (D1 and D2 in Fig. 3.5(c)), a relatively high peak voltage and a large input power are required to efficiently rectify the AC input signal. Thus, the target applications are RFID tags with a supply voltage above 2 volts and a current consumption in the mA range.

In the following rectifier design [31], the goal was to improve the efficiency at lower input voltages (compared to the previously described CMOS rectifier) such that the rectifier can be used in low-voltage systems where the supply voltage can be very small, e.g., less than one volt. The architecture in Fig. 3.7 uses a CMOS cross-connected bridge\(^2\) in combination with one active diode to both simplify the architecture and at the same time, achieve better efficiency at low input voltages. The cross-connected bridge is based on the full wave diode bridge, and the four diodes are replaced with one pair of pMOS and one pair of nMOS switches [37–39].

An active diode has been placed between the load and the output of the bridge so that the reverse current leakage, which causes the efficiency to drop for increasing input voltages in the cross-connected bridge, can be effectively eliminated. The problem with reverse leakage in the cross-connected CMOS bridge is discussed in Paper A of this thesis. As shown in Fig. 3.7, the active diode consists of a pMOS switch, M1, driven by a two-input comparator that controls the gate voltage of M1.

Additionally, two switches are shown that are connected to the bulk of M1 and that have their gates cross-connected to the output of the bridge and to the DC output. The purpose of this circuit, which was introduced in [40,41] for RFID rectifiers, is to ensure that the bulk of the pMOS transistor is always connected to the highest potential so that the parasitic vertical PNP transistor of M1 is prevented from turning on, thereby minimizing the risk for latch-up and the leakage of current to the substrate.

\(^2\)This rectifier is also known as a four transistor cell, negative voltage converter and a differential drive bridge rectifier.

![Figure 3.6: Simulated power and voltage conversion efficiency for the rectifier in Fig. 3.5(c). The figure is based on data from [30].](image-url)
This rectifier was designed using a standard 0.18 μm CMOS process and is simulated with a load of 500 Ω at the frequencies of 100 kHz and 1.5 MHz. The simulation results clearly reveal highly efficient rectification with low peak input voltages as low as 0.7 volts. However, the efficiency for this rectifier can be expected to drop for lighter loads because the power consumption of the active diode will become an increasingly larger fraction of the output power. This problem is addressed in Paper C of this thesis.

3.2.2 Threshold cancellation techniques

Several techniques have recently been proposed to improve CMOS rectifiers based on diode-connected MOS transistors (MOS diodes). The diode voltage of the MOS diode is determined by the threshold voltage of the MOS transistor which is typically 0.65 V for a pMOS diode in 0.35 μm CMOS. Naturally, a higher voltage drop compared to the Schottky diode results in a significantly lower conversion efficiency due to the increased loss in the diodes. Therefore, different threshold cancellation techniques have been developed for diode-connected MOS transistors to reduce the effective diode voltage.

![Figure 3.7: Low voltage CMOS rectifier based on the cross-connected bridge (a) and an active diode (b) [31]. Copyright © 2010 IEEE. Figure reprinted with permission.](image)

![Figure 3.8: Simulated voltage and power conversion efficiency of the rectifier in Fig. 3.7 [31]. Copyright © 2010 IEEE. Figure reprinted with permission.](image)
3.2. Recent Research in CMOS Rectifier Design

The technique utilizing \(V_{th}\)-cancellation in MOS diodes for RFID rectifiers was introduced in [28] for a simple voltage doubler rectifier based on nMOS diodes, as shown in Fig. 3.9(a). In this architecture, a bias voltage \(V_{th}\) is connected between the gate and the drain so that the effective threshold becomes \(V_{th} - V_{th}\) for each MOS diode. The output voltage can then be written as \(V_R = 2(V_{rf} - V_{th} + V_{th})\). Thus, with a bias that is approximately equal to the threshold, the DC output of the voltage doubler is increased from \(2(V_{rf} - V_{th})\) to \(2V_{rf}\). The bias voltage for each diode was implemented with a bias generator, as shown in Fig. 3.9(c). The \(V_{th}\)-generator is connected to a battery in this so-called semi-passive tag. This allows for the rectification of signal amplitudes below the threshold voltage as the threshold is cancelled by the on-chip supply voltage. To generate a DC voltage of several volts from a small input RF signal, a stacked architecture based on six unit cells (Fig. 3.9(a)) in a Dickson charge pump configuration was used. The bias voltage for each of the twelve MOS diodes was supplied from one external bias generator using switched capacitor circuits in a \(V_{th}\) distribution network. Consequently, this technique has been called external threshold cancellation (EVC) for semi-passive tags.

The technique with \(V_{th}\)-cancellation in RFID rectifiers has been further developed for a passive tag in CMOS [29, 43]. The proposed rectifier is shown in Fig. 3.10 and uses one pMOS diode \((M_{p1})\) and one nMOS diode \((M_{n2})\) with threshold cancellation in a voltage doubler architecture. Rather than using an external battery to generate the bias voltage, this architecture uses two internal bias generators that are connected to the DC output voltage. The bias circuits include a small capacitor \(C_b\) that holds the bias voltage of the MOS diodes and a large resistor \(R_b\) that limits the bias current to minimize the power dissipation. In this voltage doubler architecture where the \(V_{th}\)-cancellation is activated by the output voltage, highly efficient rectification is achieved as the output exceeds \(V_{th}\), which is the voltage required to drive the internal threshold cancellation (IVC) circuit. Consequently, the efficiency (Fig. 3.10) is initially low at the start up and then reaches a maximum. The drop in efficiency for higher input levels is caused by increased reverse

![Figure 3.9: Voltage doubler with \(V_{th}\)-cancellation (a), illustration of the rectification mechanism (b) and bias generation circuit (c) [28]. Copyright © 2006 IEEE. Figure reprinted with permission.](image-url)
leakage in the MOS diodes, which occurs when the effective threshold is reduced. In addition, as discussed in Paper B of this thesis, reducing the diode voltage in a diode-connected MOS transistor with IVC below ca. 200 - 300 mV will considerably reduce the power conversion efficiency for all input voltage levels due to the increased reverse leakage and increased bias current.

The problem with low efficiency for small input voltages in rectifiers with IVC MOS diodes has been discussed in [42]. In this paper, a self $V_{th}$-cancellation technique was proposed for a CMOS voltage doubler (Fig. 3.11) that achieves highly efficient AC to DC conversion directly at the turn-on voltage of the rectifier. The rectifier uses one nMOS transistor and one pMOS transistor that have their gates connected to the output terminal and to the ground terminal, respectively. In this configuration, the gate-source of each transistor will be actively biased from the output; thus, the effective thresholds will be reduced using a bias circuit powered by the output voltage. In the resulting

Figure 3.10: Voltage doubler in CMOS with internal threshold cancellation (IVC) [29]. The measured power conversion efficiency includes a comparison with the EVC technique described above. Copyright © 2007 IEEE. Figure reprinted with permission.

Figure 3.11: CMOS voltage doubler with self voltage cancellation (SCV). The simulated power conversion efficiency that includes a comparison with a voltage doubler based on nMOS diodes [42]. Copyright © 2007 IEEE. Figure reprinted with permission.
characteristic (Fig. 3.11), a maximum efficiency occurs when the output voltage reaches $V_{th}$ and the effective threshold of both transistors are zero. Further increasing the output voltage will bias the transistors in reverse, which results in a reverse current and a reduced efficiency. Thus, the behavior of this rectifier is similar to that of the cross-connected bridge, shown in Paper A, with a high efficiency at one input level when the output DC voltage is $V_{th}$, which is typically 0.65 V.
This chapter presents further studies of DC generation using multiple coil antennas. The studies are based on the results presented in Paper F, which is related to research question Q3, stated in Chapter 1.

Cascaded DC generation is compared to single antenna DC generation for a spherical coil antenna using three independent orthogonal windings. Additionally, a transponder architecture in CMOS that combines the FSK front-end and the architecture for cascaded DC generation presented in Paper F is included.

4.1 Cascaded DC Generation

The concept of cascaded DC generation is shown in Fig. 4.1, where the DC generation blocks are connected in series with a common storage capacitor that is charged from the outputs of each rectifier block [44]. In contrast to single antenna DC generation where two out of three DC generation blocks are unused, the cascade allows the generated DC from all blocks to be summed on a common load.

For a transponder where three orthogonal antennas with cascaded DC blocks are used to supply the chip, the cascaded DC voltage will depend on the orientation of the transponder relative to the reader. To compare single antenna DC generation to cascaded DC generation, the area of the three windings as observed from the location of a reader coil antenna can be compared: Because the area of a winding is directly proportional to the induced voltage [7], and because the induced voltage is directly proportional to the rectified output voltage (3.8), the individual area and the summed area can be calculated for this comparison. In the following analysis, the area observed from a reader coil located on the same axis and in parallel to the $z$ winding of the spherical coil antenna in Fig. 4.2a was determined. The summed area is compared to the individual area of respective windings for two different rotation directions. The calculations are briefly shown below, and the results are plotted in Fig. 4.3 and in Fig. 4.4.
Rotation around the y-axis with $\beta = 0$ degrees:

The area of windings $x$, $y$ and $z$ can be written as

\[ A_x = 0, \]  \hspace{1cm} (4.1)  
\[ A_y = \pi ab = \pi r^2 |\sin(\alpha)| \]  \hspace{1cm} (4.2)

and

\[ A_z = \pi r^2 |\cos(\alpha)| \]  \hspace{1cm} (4.3)

so that the total area is written as

\[ A_t = \pi r^2 (|\sin(\alpha)| + |\cos(\alpha)|). \]  \hspace{1cm} (4.4)

Normalizing the total area to the maximum area of one winding yields

\[ A_n = |\sin(\alpha)| + |\cos(\alpha)|. \]  \hspace{1cm} (4.5)

Rotation around the x-axis with $\alpha = 45$ degrees:

The area of windings $x$, $y$ and $z$ can be written as

\[ A_x = \pi r^2 |\sin(\beta)| \]  \hspace{1cm} (4.6)

and

\[ A_y = A_z = \pi r^2/\sqrt{2} |\cos(\beta)|. \]  \hspace{1cm} (4.7)
4.1. Cascaded DC Generation

Figure 4.2: a) Schematic figure of a spherical coil antenna with three orthogonal windings x, y and z with radii r. b) The antenna is rotated around the y-axis by $\alpha = 45$ degrees. The angle for rotation around the x-axis is $\beta = 0$ degrees. The two windings y and z appear as one as half of each winding cover each other. c) One winding (rotated around the y-axis) observed by the reader as an ellipse with the semi-major axis $a$ and the semi-minor axis $b$ respectively.

The total normalized area is given as

$$A_n = \frac{A_x + 2A_y}{\pi r^2} = |\sin(\beta)| + \sqrt{2}|\cos(\beta)|. \quad (4.8)$$

The comparisons presented in Fig. 4.3 and Fig. 4.4 show that the area observed by the reader antenna is increased by up to two times and by up to three times for the

Figure 4.3: Comparison of the total winding area (cascade) to the individual winding area (single) for rotation around the y-axis of a spherical coil antenna with three windings. The traces for cascade and single are based on (4.5) and (4.2),(4.3), respectively.
cascade in the two different rotation directions, respectively. Fig. 4.4 also shows that the maximum for which the area is three times larger occurs for $\beta \approx 35$ degrees when the areas of the three windings observed by the reader antenna are equal. Given that cascaded DC generation allows the required induced coil voltage to be reduced three times and that the decay of the magnetic field is 60 dB/decade (Fig. 3.12), the range can ideally increase up to 44 % for this orientation.
4.2 Front-end Architecture

A front-end architecture for transponders using multiple antennas is shown in Fig. 4.5. The front-end is based on the two separate architectures for FSK modulation respective cascaded DC generation, both presented in detail in Paper F. To combine these two architectures into one front-end, that utilizes the cascaded DC voltage to supply one out of three FSK modulators for transmission, six switches were added: Three pMOS switches\(^1\), driven by the EOB\(_i\) signals, and three switches for the supply to the EOB

\(^1\)Body bias was used to prevent leakage, as described for switch M11 in Fig. 3.7.
detectors. Included but not shown in the figure is one output buffer for each EOB detector, supplied by $V_{dd}$, in series with an inverter to generate the $EOB_i$ signals.

To power up the transponder front-end, an RF burst is sent from a reader, as further described in Section 3.5 and 4.1 of Paper F. When the select signal is generated, one of the three EOB detectors is activated. At the end of the RF burst, an $EOB_i$ signal is generated so that $V_{DD}$ is connected to the supply of the selected FSK modulator at the same time as the modulator is biased.

The designed front-end was simulated as described in Section 3.5 of Paper F. Here the three induced voltages and the storage capacitor were chosen 50 mV and 30 nF, respectively. The simulation results in Fig. 4.6 show that after the RF burst of 25 ms, oscillation occurs for ca. 3 ms in the selected modulator (z) with a maximum peak voltage equal to the cascaded DC voltage $V_{DD} \approx 3.6$ V.

Compared to the use of single antenna DC generation, the simulation results of the presented FSK front-end with cascaded DC generation are promising for further improving readability when tracing moving objects.
Summary of the Papers

This section briefly summarizes the papers included in this thesis. The main work in the papers was performed by the first author, except where otherwise stated.

5.1 Paper A – Improved Efficiency in the CMOS Cross-Connected Bridge Rectifier for RFID Applications

Authors: Hans Rabén, Johan Borg, Jonny Johansson
Published: Proceedings of MIXDES 2011, 18th International Conference "Mixed Design of Integrated Circuits and Systems"

This paper discusses the limitations in the well-known CMOS cross-connected bridge rectifier. An analysis is performed to illustrate the problem associated with reverse charge leakage, which limits the power conversion efficiency in this architecture. Based on this analysis, a modified cross-connected bridge rectifier is proposed using active diodes based on diode-connected MOS transistors using the internal threshold cancellation technique (ITC) and reverse leakage control. The paper includes the simulation results of the rectifier performance for LF and HF RFID applications.

5.2 Paper B – A Model for MOS Diodes with $V_{th}$-Cancellation in RFID Rectifiers

Authors: Hans Rabén, Johan Borg, Jonny Johansson
Published: IEEE Transactions of Circuits and systems II 2012

In this paper, a detailed theoretical analysis of diode-connected MOS transistors using the internal threshold cancellation technique (ITC) is presented. Equations are derived
and a model for the power conversion efficiency is developed for a bridge rectifier based on MOS ITC diodes in a given CMOS process. A design procedure is included that describes how to optimize MOS ITC diodes for maximum power conversion efficiency in a rectifier in a CMOS process.

5.3 Paper C – An Active MOS Diode with $V_{th}$-Cancellation for RFID Rectifiers

Authors: Hans Rabén, Johan Borg, Jonny Johansson
Published: Proceedings of IEEE RFID 2012

This paper presents a highly efficient active diode in CMOS for low-power RFID applications. The diode is a redesign of the active diode presented in Paper A, which uses the MOS ITC technique with reverse leakage control. A theoretical background of the problem associated with MOS ITC diodes regarding the difficulty in combining a low diode voltage with a high power conversion efficiency in a rectifier application is presented. This paper includes a detailed functional description of the proposed diode along with a simple design procedure. The simulated performance is presented for a single diode rectifier in a 0.35 μm CMOS process.

5.4 Paper D – A Discrete Model of the DC Charge-up Phase in RFID Rectifiers

Authors: Hans Rabén, Johan Borg, Jonny Johansson
Published: Proceedings of MIXDES 2013, 20th International Conference “Mixed Design of Integrated Circuits and Systems”

This paper presents a discrete model of the DC charge-up phase in the inductively coupled RFID system. The model is derived for the DC charge-up phase of the storage capacitor in the DC generation block that serves as the supply voltage of a transponder chip. Based on the derived model, a relation between the induced coil voltage and the available chip current is derived for the pulsed RFID system.

5.5 Paper E – Design of Voltage Multipliers for Maximised DC Generation in Inductively Coupled RFID Tags

Authors: Hans Rabén, Johan Borg, Jonny Johansson
Published: IEEE Transactions on Circuits and Systems I 2014
This paper presents modeling and circuit design of voltage multipliers for inductive RFID applications. Equations are derived for maximized DC generation when using voltage multipliers in combination with the resonance circuit in the inductively coupled RFID system. Circuit design and modeling of multipliers based on FTC diodes are also included. In addition, this paper includes design examples with typical coil antennas together with an analysis that shows how the voltage multiplication affects the range of the inductive RFID system.

5.6 Paper F – A CMOS Front-end for RFID Transponders Using Multiple Coil Antennas

Authors: Hans Rabén, Johan Borg, Jonny Johansson

This paper presents a front-end design for inductive RFID transponders using multiple coil antennas for reduced orientation sensitivity when tracing moving objects. The front-end uses three independent orthogonal windings in a spherical coil antenna, in which three windings are used for reception and one is used for transmission. A select function is designed to select the winding that is most favorably oriented toward the reader for transmission. The circuit design and simulation results of a front-end in CMOS for the pulsed RFID system using FSK modulation are presented in addition to an architecture for cascaded DC generation.

Contributions: Johan Borg performed the measurements on the manufactured chip and presented the measurement results in the figures as well as designed the multiple coil antenna prototype.
This thesis has focused on DC generation for passive chip RFID technology in inductively coupled systems. Specifically, the efficiency of the rectifiers in low-cost semiconductor technologies has been the target for improvements to enable additional chip functionality and reduced costs for the RFID system. The main technique discussed and included in the publications is internal threshold cancellation (ITC) in diode-connected MOS transistors. Transistor level circuit design and a thorough theoretical analysis of ITC MOS diodes were completed. Performance limitations were revealed, and an improved technique, termed full threshold cancellation (FTC), for diode-connected MOS transistors was proposed. This thesis has also demonstrated how the number of voltage multipliers in a charge pump configuration, can be chosen to achieve maximum DC generation in the inductive RFID system. Furthermore, this thesis has presented front-end circuit solutions for transponders using multiple coil antennas for reduced orientation sensitivity when tracing moving objects. In addition to the publications, the thesis also includes a theoretical model for single diode RF to DC conversion and a study of multiple coil antenna DC generation.

6.1 Conclusion

The thesis is concluded by answering the research questions stated in Section 1.1:

Q1: Can rectifiers in CMOS be made more efficient to improve the power budget of a chip to allow additional functionality?

The answer to this question is that rectifiers in CMOS can be made more efficient to improve the power budget of a chip. This concern has been the main question of this thesis and has resulted in improvements of the CMOS cross-connected bridge presented in Paper A, a design procedure to optimize CMOS rectifiers based on MOS ITC diodes presented in Paper B and an active MOS diode presented in Paper C.
Q2: Can rectifiers in CMOS replace rectifiers based on Schottky diodes that are used in advanced semiconductor processes?

The answer to this question is that rectifiers in CMOS can potentially replace Schottky diodes. The proposed MOS diode in Paper C has a simple and power efficient architecture, which makes it suitable for low-power multi-stage rectifiers, as demonstrated in Paper E.

Q3: Can multiple coil antennas be used in inductive transponders for improved DC generation as well as reduced orientation sensitivity?

The answer to this question is that transponders using a spherical coil antenna with three orthogonal independent windings can be used to reduce orientation sensitivity and for cascaded DC generation to improve the power budget of the chip, as proposed in Paper F.

6.2 Future Work

Three suggestions for future work on DC generation for inductive RFID applications are presented below:

- Increase the upper frequency limit of the FTC diode to allow for the design of voltage multipliers in CMOS for improved range and reduced costs in high-frequency (13.56 MHz) RFID applications.
- Further evaluate the use of multiple coil antennas in transponders to reduce orientation sensitivity and for cascaded DC generation in long-range inductively coupled RFID systems.
- Evaluate whether high Q coil antennas can be used in combination with a self calibration scheme of the resonance frequency to allow maximization of the voltage gain in the resonance circuit of an inductive RFID transponder.


Part II
Improved Efficiency in the CMOS Cross-Connected Bridge Rectifier for RFID Applications

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Improved Efficiency in the CMOS Cross-Connected Bridge Rectifier for RFID Applications

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Abstract
A bridge rectifier based on the cross-connected NMOS-PMOS bridge that avoids the inherent degradation of power conversion efficiency for increasing input levels is presented. Instead of PMOS switches, the proposed rectifier uses diode-connected MOS transistors with static threshold cancellation and minimised diode reverse leakage. With a simple and power efficient circuit solution the new rectifier allows for low-power, passive tag implementation in standard CMOS for both LF and HF RFID applications. Simulation results of the proposed rectifier in a 0.35 μm CMOS process show a power conversion efficiency over 60% for all input levels above 0.75 V with a 100 kΩ load and an input signal frequency of 13.56 MHz. The simulated DC output voltage at the same conditions is approximately $V_{\text{out}} = 0.3$ V. A model for the PCE of the new rectifier that includes the impact of the $V_{\text{th}}$-generator is developed and compared with simulated results.

1 Introduction
In passive RFID, the ability of the DC-generating block to efficiently convert a weak incoming RF-signal to a stable power supply with enough current to support a complex chip is one of the keys in meeting future demands on RFID technology. These demands include lower cost, higher security and commutation at higher rates and longer reading ranges as well as on chip integration of sensors for environmental monitoring [1]. There are many factors that limit the rectifier performance and power extraction for wireless powered devices. For efficient use of available RF input power, the rectifier is required to have a low turn-on voltage to minimise the dead zone where all input power is wasted. The turn-on voltage directly depends on the threshold of the active devices used, such as MOS diodes, Schottky diodes, low-$V_{\text{th}}$ and floating gate transistors [2] [3]. A second important limitation is the reverse leakage of these devices that reduces power conversion efficiency after the rectifier is activated.

In this work, a bridge rectifier based on the NMOS-PMOS cross-connected bridge rectifier (cc-bridge) is presented in which the degradation due to reverse leakage is effectively minimised. The PMOS pair of the cc-bridge is exchanged for MOS diodes to avoid the inherent charge leakage. Two active inverters and a $V_{\text{th}}$-generator are added to improve the function of the MOS diodes.

The function of the cc-bridge is described in section 2.1. In section 2.2, the problem with charge leakage is described and related work is presented. The circuit design, pre-
Figure 1: The conventional full wave diode bridge (a) and the NMOS-PMOS gate cross-connected bridge (b).

2 The Cross-Connected Bridge

2.1 Principle

As a background to the proposed rectifier the principle of the cc-bridge is presented. The cc-bridge in Fig. 1 is developed from the conventional full wave diode bridge where the diodes have been replaced with switches. During the rectifying operation, the switches conduct in pairs, \( M_p2 \rightarrow M_n1 \) and \( M_p1 \rightarrow M_n2 \); thus, the current to the load will have the same direction during both the positive and negative phases of the input signal (see also Fig. 3). Because each switch is driven by the full input swing, the rectifier minimum turn-on voltage becomes \( V_{th} \), and the developed DC voltage across the load capacitor ideally becomes \( V_{AC} - 2V_{DS} \), where \( V_{AC} \) is the peak value of the input signal and \( 2V_{DS} \) is the drain-source voltage drop on the conducting pair connecting the voltage source and the load. The advantages of using a switched structure compared to a bridge with conventional diodes are reduced minimum turn-on voltage and higher output voltage for the same input swing [4]. The cc-bridge achieves high power conversion efficiency (PCE) at low input signal levels, which has made this structure relevant for low-power and long reading range RFID applications. However, the switched structure suffers from a known problem with reverse charge leakage that severely reduces its PCE for input voltages above a certain level as simulated in Fig. 2. This leakage occurs during the on-off transition when a switching pair conducts in reverse for a short period of time, as described in more detail in section 2.2. As indicated in Fig. 2, the problem with reverse
2. The Cross-Connected Bridge

2.0.4

0.6
0.8
1
1.2
1.4
1.6
1.8
2

0
10
20
30
40
50
60
70
80

Vin (V)

PCE (%)

RL100k

RL2k

Figure 2: PCE of the cc-bridge at two different loads simulated at an input signal frequency of 13.56 MHz. Less degradation of PCE can be seen with a heavier load because the loss due to leakage becomes smaller compared with the output power.

charge leakage is more pronounced for a light load and thus for RFID chips with low power consumption.

2.2 Reverse charge leakage

As seen in Fig. 2 the cc-bridge reaches a peak in efficiency at relatively low input levels. This has been explained as a result of reverse charge leakage from the output capacitor when the input swings below the DC output level. During this time interval, when one of the output transistors should be completely turned off, its drain and source will interchange and current will flow toward the input, creating additional power loss in the NMOS and PMOS transistors. To investigate this phenomenon in more detail, we consider the cc-bridge during half a period of the input signal when \( M_{p1} \) and \( M_{n2} \) are on and \( M_{p2} \) and \( M_{n1} \) are off. The resulting structure is shown in Fig. 3. From the simplified cc-bridge we have the conditions for leakage expressed as

\[
V_{th2} < V_H < V_{out}
\]

and

\[
V_{out} - V_L > V_{th1}.
\]

When these conditions are fulfilled, both \( M_{p1} \) and \( M_{n2} \) are biased in reverse, which results in leakage, as shown in the simulation in Fig. 4. As a result, the maximum output voltage possible without leakage in the cc-bridge, is for \( V_{DC} = V_{th1} \) which is typically 0.7 V in 0.35\( \mu \)m CMOS.
An alternative structure replacing only one pair of diodes with MOS switches avoids this problem because the remaining diode pair does not conduct in reverse (except the small leakage current) as the switches do here. However, this structure will suffer from the higher voltage drop of the remaining diodes. Several works address the problem of reverse charge leakage in the cc-bridge for RFID applications. In [5], a detailed analysis shows the PCE and its peak characteristics for the cc-bridge mathematically. A new bootstrapping technique is used in [6] to eliminate the threshold voltage of diode-connected MOS transistors that are then introduced in simulations instead of the output PMOS pair. Recently, in [7], comparators are used in the cc-bridge to control the reverse leakage in the output PMOS pair resulting in improved voltage conversion efficiency, while PCE is not reported. In [8], the NMOS pair in the cc-bridge is replaced with active diodes. These diodes are realised with NMOS switches driven by high-speed comparators with extremely fast switching, which eliminates reverse leakage and achieves a power conversion efficiency greater than 80% for higher input levels. One of the remaining problems in [8], indicated by the presented results, is that the PCE is low for input signals up to 1.5 V. This problem has been addressed in a recent work [9] where a comparator-driven, low voltage switch is placed between the load and the output of the cc-bridge to eliminate the reverse leakage. This result in a PCE greater than 80% for input voltages from 0.7 V to 1.8 V at a frequency of 1.5 MHz and a load of 500 Ω. However, both of the works in [8] and [9] are limited to applications with chip power consumption in the mW range because of the use of relatively power hungry comparator-driven switches to control the reverse leakage.

In the current work, a less power-hungry rectifier architecture, using active diodes to control the reverse leakage, resulted in comparable power conversion efficiency, both in the mW and μW range, as well as for LF and HF RFID applications.

Figure 3: The simplified schematic of the cc-bridge during the positive phase of the input signal when $M_{p2}$ and $M_{n1}$ are off.
Figure 4: Transient analysis showing the reverse charge leakage in switch $M_{p1}$ during one period of the input signal with an amplitude of 0.9 V. Two negative current pulses occur for $I_{D1}$ each time the switch turns on, the first starting when the difference between $V_{out}$ and $V_L$ equals $V_{th1}$ and continues until $V_H$ equals $V_{out}$.

3 Circuit Design

In the proposed rectifier, the leaking PMOS switches in the cc-bridge are replaced with diode-connected PMOS transistors with static threshold cancellation. This section starts with a short description of static $V_{th}$-cancellation before introducing this technique in the design of the proposed rectifier. The impact of the $V_{th}$-generator on efficiency is analysed and included in a model for the PCE of the rectifier.

3.1 Static Threshold Cancellation

Using diode-connected MOS transistors in rectifiers has the disadvantage of low power conversion efficiency and higher turn-on voltage due to the voltage drop of $\approx V_{th}$ from source to drain. For low voltage applications, such as RFID rectifiers, Schottky diodes or low voltage-drop transistors can be used in advanced CMOS processes at an additional cost. In standard CMOS, a static threshold cancellation technique has been used for diode-connected MOS transistors to improve the PCE for RFID rectifiers [10] [11]. A simple illustration of this technique is shown in Fig. 5 (a) for a PMOS transistor. In contrast to a diode-connected MOS transistor where $V_{SD} = V_{th} + V_n$, the threshold drop from source to drain is cancelled with an additional diode-connected transistor that is forward biased from drain to gate of M1, so that $V_{SD}$ becomes

$$V_{SD} = V_{in} - V_{out} = V_{in} - (V_{in} - V_{SG1} + V_{SG2}) = V_{o1} - V_{o2}$$

(3)

where $V_{o1}$ and $V_{o2}$ are the overdrive voltage of transistor M1 and M2 respectively. The
concept with static threshold cancellation can be adapted easily in the cc-bridge by replacing $M_{p1}$ and $M_{p2}$ with PMOS diodes because the drain of PMOS will be connected to the output voltage so that the $V_{th}$-generating diode will be forward biased. One problem with using static threshold cancellation MOS diodes comes from reverse leakage current that reduces the efficiency of the rectifier [8]. With the drain-gate fixed to $V_{th}$, the output transistor $M1$ will be biased in reverse when $V_{in} < V_{out}$, resulting in leakage in the off-state. In next section a simple technique that use inverters [12] to minimises this leakage is presented.

3.2 The proposed rectifier

The proposed modification of the cc-bridge is shown in Fig. 6. Here, the cross-connected PMOS switches are replaced by PMOS diodes with $V_{th}$-cancellation in combination with two standard PMOS-NMOS inverters, $I1$ and $I2$. The purpose of the inverters is to turn the diodes off completely during half of a cycle to minimise diode reverse leakage, as illustrated in Fig. 7. Each inverter has its negative supply connected to the $V_{th}$-generating diode $M_{p3}$ and its positive supply connected to the output so that the gates of $M_{p1}$ and $M_{p2}$ are connected to either $V_{b}$ or $V_{out}$. During the positive phase of the input signal, the negative supply of $I1$ connects to the gate of $M_{p1}$ so that its drain-gate voltage equals $V_{th}$ and the static threshold cancellation is activated. Similarly, during the negative phase of the input signal, the positive supply connects to the gate so that the drain-gate voltage is zero and the reverse leakage is minimised. In the design of the rectifier, the widths of $M_{n1}$, $M_{n2}$, $M_{p1}$ and $M_{p2}$ were optimised for both loads (35μm and 200μm for 100 kΩ and 2 kΩ, respectively) to achieve maximum power and voltage conversion efficiency. The inverters were optimised for maximum speed by minimizing channel widths of the NMOS-PMOS pair. Bias current in the $V_{th}$-generator was minimised by the proper choice of $R_b$ as to limit power loss when the output voltage increases. In the critical case with
Figure 6: Proposed rectifier. The leaking PMOS switches of the cc-bridge are replaced by diode-connected PMOS transistors with $V_{th}$ cancellation in combination with inverters for minimized diode reverse leakage, to achieve both low turn on voltage and improved efficiency.

low output power (100 kΩ load), when the loss in $R_b$ becomes a larger fraction of output power, calculations show that the degradation of PCE due to the $V_{th}$-generator is below 7% for input voltages up to 2 V.

3.3 Power conversion efficiency

The efficiency of the cc-bridge have been analysed in [5] where loss in the NMOS and PMOS switches together with the impact of the reverse charge leakage as well as substrate loss is included. For the proposed rectifier, where the PMOS switches are replaced with diodes to avoid reverse charge leakage, the analysis below include loss in the PMOS diodes together with the loss due to the the $V_{th}$-generator, which are the main contributors to the loss, while loss in the NMOS switches as well as substrate loss can be neglected. Since the PMOS diode reverse leakage is minimised in proposed rectifier it is also neglected while the loss in the two inverters are neglected to simplify the analysis.

The efficiency of the cc-bridge with static threshold cancellation can be written as

$$PCE = \frac{P_{out}}{P_{out} + P_{loss}} \approx \frac{P_{out}}{P_{out} + P_{V_t} + P_{M1}}$$

where $P_{out} = \frac{V_{out}^2}{R_L}$. In order to achieve a useful expression of PCE, the output voltage is here approximated as $V_{out} = \hat{v}_{in} - \hat{v}_{SD} \approx \hat{v}_{in} - 0.3$ V. The loss due to the $V_{th}$-generator is given by

$$P_{Vt} = P_{M2} + P_{R2} \approx I_b V_{th} + \left(\frac{V_{out} - V_{th}}{R_b}\right)^2 = \frac{V_{out} (V_{out} - V_{th})}{R_b}$$

(5)
From Fig. 5 (b) the loss due to the current pulse in M1 can be derived as below [13]:

$$P_{M1} \approx \frac{2}{\pi} \int_{\phi_1}^{\pi/2} (\hat{v}_{in} \sin(\phi) - \hat{V}_{out}) \hat{i}_{D} \frac{\phi - \phi_1}{2 - \phi_1} \, d\phi$$  

(6)

where $\phi_1 = \sin^{-1}(\frac{\hat{V}_{out}}{\hat{v}_{in}})$. To find the peak current the input and output charge is written as

$$Q_{in} \approx \frac{1}{2} \hat{i}_{D} T_1 = \frac{1}{2} \hat{i}_{D} \left( \frac{\pi}{2} - \phi_1 \right)$$  

(7)

and

$$Q_{out} = I_{out} T_2 = \frac{\hat{V}_{out} \pi}{R_L}$$  

(8)

$$Q_{in} = Q_{out} \rightarrow \hat{i}_{D} = \frac{\hat{V}_{out}}{R_L} \frac{\pi}{\frac{\pi}{2} - \phi_1}$$  

(9)

The resulting PCE is plotted in Fig.8 for $R_L = 100k\Omega$ and $R_b = 300k\Omega$. Simulations showed that the discrepancy between the modelled and simulated efficiency is mainly due to the loss in the two inverters which were neglected in the model.

### 4 Simulation Result

The proposed rectifier was designed and simulated in a 0.35 μm CMOS process. In order to verify performance in both the μW and mW range of chip power consumption, the rectifier was designed in two different versions. The power conversion efficiency was simulated based on the following equations:
4. Simulation Result

Figure 8: PCE of proposed rectifier simulated with two different loads at 13.56 MHz.

\[
PCE = \frac{P_{\text{out,DC}}}{P_{\text{in,RF}}} = \frac{V_{\text{out}}^2}{R_L} * \frac{P_{\text{out}}}{R_L} = \frac{V_{\text{out}}^2}{R_L} \times \frac{P_{\text{in,RF}}}{R_L}
\]  

(10)

where \(P_{\text{in,RF}} = \frac{1}{T} \int_{0}^{T} V_{\text{in}}(t) \times I_{\text{in}}(t) \, dt\)

(11)

The PCE of the proposed rectifier shown in Fig. 8 clearly reveals the improvement after eliminating the charge leakage in the cc-bridge. Instead of fast degradation with increasing input levels, the efficiency is almost constant at the maximum efficiency. Comparing Fig. 2 and Fig. 8, the cc-bridge shows about 10% higher peak efficiency around \(V_{\text{in}}=0.8\) V with a load of 100 kΩ. This result can be explained as incomplete \(V_{\text{th}}\)-cancellation at low output voltages for the proposed rectifier while the cc-bridge has zero reverse charge leakage. Simulations with \(V_{\text{in}}\) from 2 V up to the oxide breakdown voltage 3.6 V showed a maximum power conversion efficiency of 70% for \(R_L=2\) kΩ, and remained almost unchanged for \(R_L=100\) kΩ. The output voltage characteristics in Fig. 9 and Fig. 10 show that the proposed circuit and the cc-bridge has comparable voltage conversion efficiency for both loads. A simulation of the power dissipation in the rectifier was performed with a load of 100 kΩ and \(V_{\text{in}}\) 1.5 v. At an input power of 19.8 \(\mu\)W the power developed in the load was 13.1 \(\mu\)W. The loss in the PMOS pair, the two inverters and \(R_b\) was 4.5 \(\mu\)W, 1.2 \(\mu\)W and 1.0 \(\mu\)W respectively. The loss in the NMOS pair and the loss due to body leakage was negligible.

The two different versions of the proposed rectifier was also optimized and simulated at 125 kHz to evaluate performance for LF applications. As expected both rectifiers showed slightly improved performance where the proposed rectifier has an average efficiency around 75% up to \(V_{\text{in}}\) 2 V for both loads. Simulations with \(V_{\text{in}}\) from 2 V up to 3.6 V showed a power conversion efficiency reaching a maximum above 80% for \(R_L\) 2 kΩ,
and remained almost unchanged for $R_L \ 100 \ \text{k}\Omega$. The output voltage for the proposed circuit, compared to the operation at 13.56 MHz, showed an improved linear characteristic instead of the weak dip around 1.3 V shown in Fig. 10. This improvement is a result of better inverter performance at lower frequencies.

## 5 Conclusion

In this work, a rectifier circuit based on the cc-bridge is presented that avoids reverse charge leakage and the resulting degradation of PCE with increasing input levels. The output PMOS pair in the cc-bridge is replaced with MOS diodes that employ static threshold cancellation in combination with minimised diode reverse leakage. A model for the power conversion efficiency of the proposed rectifier is developed and compared with simulations. The main advantage of this rectifier compared with earlier works is a simpler structure and high PCE from low to high input levels and without degrading rectifier sensitivity. A one-stage rectifier with a load of 100 kΩ generates a DC voltage in the range of 0.5 to 3.3 V at an efficiency above 60%. Instead of cascading bridges at their peak efficiency when generating the desired supply voltage, the proposed rectifier may be used to achieve a more robust overall DC voltage regulation system.

## 6 Acknowledgements

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Figure 10: The simulated output voltage of the proposed rectifier at 13.56 MHz.

Figure 11: Layout of the proposed rectifier.

References


A Model for MOS Diodes with $V_{th}$-Cancellation in RFID Rectifiers

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A Model for MOS Diodes with $V_{th}$-Cancellation in RFID Rectifiers

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Abstract

A theoretical model for diode-connected MOS transistors with threshold cancellation technique is developed. The model is based on a detailed analysis of the technique with internal threshold cancellation (ITC) and reveals design insight and performance limitations. Derived design equations illustrate the trade-off between the voltage drop and the reverse leakage of the diode. Furthermore, a design procedure for optimization of the power conversion efficiency (PCE) of a bridge rectifier with ITC MOS diodes was developed based on the model. A rectifier was designed and implemented in an AMS 0.35 μm CMOS process and Cadence simulation results of the PCE and the voltage conversion efficiency show good agreement with the model.

1 Introduction

In low-voltage and low-power applications, such as passive RFID, diodes with low leakage and a low turn-on voltage are necessary to achieve high efficiency. Schottky diodes or low $V_{th}$-transistors and other techniques available in advanced CMOS processes can be used at an additional cost [1] [2]. In standard CMOS processes, different threshold cancellation techniques have been proposed for diode-connected MOS transistors to improve the power conversion efficiency (PCE) of RFID rectifiers. In [3], an external $V_{th}$-cancellation technique was introduced for semi-active tags. The internal threshold cancellation (ITC) technique that uses the DC-output voltage of the rectifier to bias the gates was presented in [4]. In the self $V_{th}$-cancellation (SVC) scheme [5], the output voltage is used for improved rectification with diode-connected MOS transistors for passive tags. There are, however, few existing models for RFID rectifiers that provide useful equations for design and optimization. Recently, a detailed analysis was conducted for a simple MOS diode in RFID rectifiers in [6].

This work presents a theoretical analysis of the ITC technique for MOS diodes. Based on the analysis, a model for the PCE was developed, and a design procedure for bridge rectifiers using MOS diodes with ITC was derived. To verify the model, a bridge rectifier was designed and simulated using AMS 0.35 μm CMOS technology.

In section 2 of this paper, the diode-connected MOS transistor with ITC technique is analyzed. Section 3 presents a bridge rectifier built using ITC MOS diodes, and a model for the PCE of this rectifier is derived, including a design procedure. The results from
2 Internal Threshold Cancellation

Rectification using a PMOS transistor with and without ITC is shown in Fig. 1(b) and Fig. 1(a), respectively. The I-V characteristics of both circuits are shown in Fig. 1. In contrast to the diode-connected MOS transistor, in which $V_{SD} = V_{th} + V_{o}$, the threshold drop from source to drain in the ITC circuit is cancelled with an additional diode-connected transistor, M2, which is forward biased. The $V_{SD}$ of the MOS diode with ITC in Fig. 1(b) can be written

$$V_{SD} = V_{in} - V_{out}$$  \hspace{1cm} (1)

where

$$V_{out} = V_{o1} - V_{SG1} + V_{SG2}.$$  \hspace{1cm} (2)

Thus, $V_{SD}$ becomes

$$V_{SD} = V_{SG1} - V_{SG2} = V_{o1} + V_{th} - V_{SG2}$$  \hspace{1cm} (3)

where $V_{o1}$ is the overdrive voltage of M1. Thus, the voltage drop for the MOS diode with ITC is determined by the difference in the gate bias between M1 and M2. The condition required for the bias voltage $V_{SG2}$ to achieve partial to full threshold cancellation of M1 is

$$0 \leq V_{SG2} \leq V_{th}.$$  \hspace{1cm} (4)
2. Internal Threshold Cancellation

Figure 2: I-V characteristics of the MOS diodes in Fig. 1. The widths of the MOS diode ITC (M1) and the MOS diode (M3) are 10 μm, and the width of the Vth-generator (M2) is 5 μm. All transistors lengths are 0.35 μm.

Substituting (4) into (3) yields

\[ V_{SD1} \geq V_{o1}. \]  

Thus, M1 is always operating in the saturation region.

The forward current of a PMOS transistor in saturation can be written

\[ I_D = \frac{\beta}{2}(V_{SG} - V_{th})^2 \]  

where \( \beta \) is the MOS gain factor \( \mu pC_{ox}\frac{W}{L} \) [7]. After combining (1) and (3) with (6) and substituting \( V_{o1} \) with \( \hat{V}_{in1} \), the forward peak current of M1 becomes

\[ \hat{I}_{D1} \approx \frac{\beta_1}{2} (\hat{V}_{in1} - V_{out} + V_{SG2} - V_{th})^2. \]

An expression for the output voltage \( V_{out} \) is found by deriving the charge that is transferred into and out of the circuit in Fig. 1(b). For a sinusoidal input signal as shown in Fig. 3, the charge can be written

\[ Q_{in} \approx \hat{I}_{D1} (\frac{\pi}{2} - \phi_1) \]  

and \[ Q_{out} = (I_{out} + I_b)\pi \approx I_{out}\pi \]

provided that \( I_b << I_{out} \), as required for low-power operation. At steady state,

\[ Q_{in} = Q_{out} \rightarrow \hat{I}_{D1} = I_{out} \frac{\pi}{2} - \phi_1 \]
where the conduction angle $\phi_1$ is given by

$$\phi_1 = \sin^{-1}\left(\frac{V_{\text{out}}}{V_{\text{in}}}ight).$$  (11)

Combining (7) and (10), the drain to source voltage of M1 can be written

$$\hat{V}_{SD1} = \hat{V}_{in1} - V_{\text{out}} \approx \sqrt{\frac{2\pi I_{out}}{\beta_1}} \frac{1}{\sqrt{2}} + V_{th} - V_{SG2}. \quad (12)$$

With transistor M2 operating in the subthreshold region ($V_{SG2} \leq V_{th}$), $V_{SG2}$ is derived from the equation for the saturated current in weak inversion

$$I_b \approx I_s e^{\frac{V_{SG2} - V_{th}}{nU_T}} \quad \text{where} \quad I_s > 10I_b, \quad (13)$$

and where $I_b$ is the drain current of M2 and $I_s$ is the specific current given by $2n\beta_2 U_T^2$ [8]. The slope factor $n$ ranges from 1.2 to 1.6 for bulk CMOS devices, and the thermal voltage $U_T$ is 26 mV at room temperature. Solving (13) for $V_{SG2}$ yields

$$V_{SG2} = V_{th} - nU_T \ln \left(\frac{I_s}{I_b}\right). \quad (14)$$

Analyzing equations (11) together with (12) for a peak input voltage up to approximately 2V at a nominal $V_{out} \approx \hat{V}_{in} - 0.3V$, shows that the square root term with $\phi_1$ is close to one. The output voltage can then be approximated as

$$V_{out} \approx \hat{V}_{in} - \sqrt{\frac{2\pi I_{out}}{\beta_1}} - nU_T \ln \left(\frac{I_s}{I_b}\right) \quad (15)$$

![Figure 3: Illustration of the drain forward current in MOS diode with ITC. Here a triangular approximation of the current is used to simplify the model for low power applications [6]. The on-state of the diode lies in the interval from $\phi_1$ to $\pi - \phi_1$ when the input signal is larger than the DC output voltage.](image)
where the middle term of the equation is an approximation of the gate overdrive voltage of M1 according to (1), (3) and (14).

The primary limitation of using ITC MOS diodes in RFID rectifiers is the reverse leakage current, which reduces the efficiency of the diodes [5] [9]. The leakage occurs when $V_{SD1} < 0$, as shown in Fig. 1, and is usually several orders of magnitude larger than the leakage of a simple MOS diode. Increasing the bias current shifts the curve left, toward full cancellation, and downwards increasing the leakage. An expression for the leakage current can be derived based on Fig. 4, which shows the MOS diode with ITC and the currents in the off-state. Clearly, with the gates connected to one another, M1 and M2 combined with $R_b$ form a simple PMOS current mirror. When the input voltage $V_{in}$ swings below the output voltage $V_{out}$ the leakage current $I_{L0}$ mirrored from M2, without accounting for channel length modulation, becomes

$$I_{L0} = I_b \frac{W_1}{W_2},$$

(16)
where $W_1$ and $W_2$ are the widths of $M_1$ and $M_2$, respectively, while the channel lengths are the same for both transistors. The bias current $I_b$ can thus be written

$$I_b = V_{in} - V_{SG1} \approx \frac{\sqrt{2 \pi I_{out} - V_{th}}}{R_b}.$$  \hspace{1cm} (17)

Accounting for channel length modulation\(^1\) in $M_1$, the leakage current becomes

$$I_L = (1 + \lambda V_{DS1}) I_{Lo} = I_{Lo} + \lambda (V_{out} - V_{in}) I_{Lo}.$$  \hspace{1cm} (18)

As shown in the above equations, $I_L$ strongly depends on the widths of $M_1$ and $M_2$. Thus, by increasing the width of $M_2$, $I_L$ is reduced. The design challenge of achieving a low forward voltage drop and minimized leakage remains, as illustrated in Fig. 3. The effect of the leakage is further discussed and analyzed in section 3.

### 3 Bridge Rectifier with ITC

The concept of internal threshold cancellation can be applied to the well-known cross-connected (cc) bridge [10] [11]. In the work presented here the PMOS switches of the cc-bridge are replaced with PMOS diodes and ITC, as shown in Fig. 6. In this architecture, the gates of $M_{p1}$ and $M_{p2}$ are connected, and the output transistors share the same $V_{th}$-generator. Alternatively, the NMOS switches can be replaced with NMOS ITC [4], in the same manner with their gates connected, sharing one $V_{th}$-generator.

\(^1\)In applications in which short-channel effects become critical additional reverse leakage can be expected due to the DIBL effect.
3. Bridge Rectifier with ITC

3.1 Power conversion efficiency

The efficiency of the cc-bridge has been analyzed in [12]. There, NMOS and PMOS switch losses, substrate loss due to parasitic capacitances to the substrate, and the impact of the reverse charge leakage are included. In this work where the cross-connected PMOS switches are replaced with diodes to avoid reverse charge leakage, the analysis below includes the PMOS diode losses and loss in the \( V_{th} \)-generator. The NMOS transistor and substrate losses are neglected.

The efficiency of the bridge rectifier with MOS ITC diodes (Fig. 6) can be written as

\[
PCE = \frac{P_{out}}{P_{out} + P_{loss}} \approx \frac{P_{out}}{P_{out} + P_{Vth} + P_{on} + P_{off}}.
\]

(19)

Here,

\( P_{out} \)

The power dissipated in the load is

\[
P_{out} = I_{out} V_{out}
\]

(20)

\( P_{Vth} \)

The power consumed by the \( V_{th} \)-generator is given by

\[
P_{Vth} = P_{Mth} + P_{Rth} = I_b V_{out}
\]

(21)

\( P_{on} \)

Based on the triangular approximation in Fig. 3, the loss due to the forward current in the PMOS pair can be written

\[
P_{on} \approx \frac{2}{\pi} \int_{\phi_1}^{\pi/2} (\dot{V}_{th} \sin(\phi) - V_{out}) \hat{I}_{D1} \frac{\phi - \phi_1}{\frac{\pi}{2} - \phi_1} d\phi
\]

(22)

where \( \hat{I}_{D1} \) is given by (10). Solving the integral gives the loss as

\[
P_{on} \approx \frac{8I_{out}}{\pi - 2\phi_1} [\hat{V}_{in} - V_{out}(\frac{\pi^2}{8} + 1 + \frac{\phi_1^2}{2} - \frac{\pi}{2} \phi_1)].
\]

(23)

\( P_{off} \)

The loss due to reverse leakage in \( M_{p1,2} \) can be analyzed based on Fig. 7. Here, the bridge rectifier in Fig. 6 is driven by a sinusoidal input signal. The reverse leakage in the off-state when \( V_{DS1} > 0 \) is clearly observed in the figure including the effect of channel
length modulation on the reverse current. As a linear approximation of (16) and (2), the current in the interval when $V_{DS_1} = V_{out}$ can be written as

$$I_{L_0} \approx (1 + \lambda V_{out})I_{L_0}.$$  

(24)

The current in the interval when $0 < V_{DS_1} < V_{out}$ can then be written as

$$I_{L_0} \approx \frac{I_{L_0} - I_{L_0}}{\phi_1} + I_{L_0} \approx I_{L_0} \phi_1 \phi_1 + I_{L_0}$$

(25)

where the second approximation is valid for large input amplitudes. Based on Fig. 7, the loss then becomes

$$P_{off} \approx \frac{1}{2\pi} \left[ \int_{0}^{\phi_1} U_{out} \phi I_{L_2} d\phi + \pi V_{out} I_{L_0} \right].$$

(26)

After substituting (24) and (25) into (26), the loss due to the reverse current can be written as

$$P_{off} \approx (\phi_1 \frac{1}{3\pi} + \frac{1}{2})V_{out}(1 + \lambda V_{out})I_{b} \frac{W_1}{W_2}.$$  

(27)

The resulting equation (22) for the PCE is located at the bottom of next page.

### 3.2 Rectifier design

A design procedure that determines the optimal component values of the IVC MOS diode is developed based on the derived model (22). The design procedure targets the
maximum PCE in the rectifier bridge with IVC MOS diodes (Fig. 6) for a given load current $I_{\text{out}}$ and output voltage $V_{\text{out}}$. The three unknown design variables are $W_1$, $W_2$ and $I_b$, where $W_1$ is the width of the two output PMOS transistors $M_{p1,2}$ and $W_2$ is the width of the $V_{th}$-generator $M_{p3}$. As shown in (16) the channel lengths are chosen equal for all transistors. The design variables are determined in the procedure below based on (22) where $\phi_1$ and $\hat{V}_{\text{in}}$ are substituted from (11) and (15).

An analysis of $PCE(W_1)$ showed that the PCE has a maxima for a value of $W_1$ that is linearly dependent on $I_{\text{out}}$ but is independent of $I_b$, $V_{\text{out}}$ and $W_2$ as illustrated in Fig. 8. Based on these observations a design procedure is outlined as follows:

1. $I_b$: The bias current is chosen as low as possible to maximize PCE. A rough estimate of the smallest realizable bias current is given by $I_b \approx (V_{\text{out}} - V_{\text{th}})/R_b$ where the value of $R_b$ is limited by the allowed chip area.

2. $W_1$: The optimal value of $W_1$ is given at the maxima of $PCE(W_1)$ based on equation (22). The PCE is calculated with $I_{\text{out}}$ according to the specification. Because the result for $W_1$ is not affected by $W_2$, a recommendation is to choose $W_2 = W_1$ in the

$$PCE \approx \frac{100}{1 + \frac{I_{\text{out}}}{V_{\text{out}}(\frac{V_{\text{in}}}{\pi} - 1 + \frac{\phi_1}{2} + \frac{1}{2})} + \frac{\hat{V}_{\text{in}}}{V_{\text{out}}(1 + \lambda V_{\text{out}})W_1 W_2}}$$ \hspace{1cm} (28)
numerical evaluation of $PCE(W_1)$, for this step.

(3) $W_2$: The width $W_2$ is given at the maxima of $PCE(W_2)$ when calculated with the chosen values of $W_1$ and $I_b$ from steps (1) and (2) above. An example of an evaluation is shown on the right-hand side of Fig. 9.

(4) $R_b$: Given the chosen values of $W_1$, $W_2$ and $I_b$ the resistor value $R_b$ is calculated from (15) and (17).

4 Results

To verify the agreement between the developed theoretical model and the circuit simulations, a bridge rectifier was designed using AMS 0.35 $\mu$m CMOS technology and simulated using Cadence Spectre. The circuit was designed according to the described design procedure in Sec. 3.1, for maximal PCE at an output voltage of 1.5 V at a load current of 15 $\mu$A. The resulting component values are shown in Table 1. The width of the NMOS switches ($W_{n1,2}$) was selected to be 140 $\mu$m so that their on-resistance was low enough to have a negligible impact. All transistors were chosen with the minimum channel length 0.35 $\mu$m.

Equation (22) was evaluated and plotted in Matlab for comparison with the simulated results as shown in Figs. 9 and 10. The two graphs in Fig. 9 show that the simulated efficiency has a maximum at the optimal values for $W_1$ and $W_2$ as predicted by the design procedure. While the simulation predicted a slightly higher optimal value for $W_1$ (left), the maxima for $W_2$ (right) agrees well with the model. In both graphs, the model overestimates the efficiency by 2 – 3%. This deviation (also observed for the PCE in Fig. 10) can possibly be attributed to approximations made in the derivation of the PCE model, resulting in an underestimation of the loss. In Fig. 10, the voltage conversion efficiency (VCE) and the PCE are simulated for comparison with the model. Both show good agreement between the simulations and the model.

<table>
<thead>
<tr>
<th>$V_{out}$</th>
<th>$I_{out}$</th>
<th>$W_1$</th>
<th>$W_2$</th>
<th>$I_b$</th>
<th>$R_b$</th>
<th>PCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5 V</td>
<td>15 $\mu$A</td>
<td>101 $\mu$m</td>
<td>19 $\mu$m</td>
<td>0.25 $\mu$A</td>
<td>4.2M$\Omega$</td>
<td>83.7%</td>
</tr>
</tbody>
</table>

The on-resistance for the NMOS switches was approximated by $R_{on} \approx 1/\beta(V_{gs} - V_{th})$ based on the drain current in the linear region [7].
5. Conclusion

The technique utilizing ITC for MOS diodes was analyzed, and a model of the PCE for a bridge rectifier was derived. On the basis of the model, a design procedure for the rectifier was developed. The optimal component values of the ITC diodes are derived for the bridge rectifier to achieve maximum PCE for a given output voltage and load current. A verification of the design procedure showed that the derived optimal component values agreed well with the simulations. Using the presented design procedure, a bridge rectifier was designed and simulated at 13 MHz in a low cost, standard CMOS process. The designed rectifier bridge achieved highly efficient DC-supply generation for low-power RFID applications with input currents in the μA range.
6 Acknowledgements

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References


An Active MOS Diode with $V_{th}$-Cancellation for RFID Rectifiers

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An Active MOS Diode with $V_{th}$-Cancellation for RFID Rectifiers

Hans Rabén, Johan Borg and Jonny Johansson

Abstract
An active MOS diode for low voltage and low power RFID rectifiers is presented. The diode is based on the technique with internal threshold cancellation (ITC) for MOS diodes and uses a simple control scheme to minimize the diode reverse leakage so that full threshold cancellation is achieved. A theoretical background that illustrates the limitations with the ITC diode and a detailed presentation of the proposed diode with a short design procedure is included. The proposed diode is implemented in AMS 0.35 $\mu$m CMOS and simulated in Cadence Spectre in a single diode rectifier. With a diode voltage ranging from 50 to 100 mV, the proposed diode simultaneously demonstrates improved voltage and power conversion efficiency of more than 20 % each for frequencies up to 1 MHz, as compared to the MOS diode with internal threshold cancellation.

1 Introduction
The rapid development of radio frequency identification (RFID) technology has led to a large area with applications; supply chain management, access control and environmental monitoring are a few important examples where RFID systems are used today. In the typical passive RFID system, a tag is remotely powered from a reader unit that transmits a radio frequency signal. In low frequency systems, 125 kHz, and high frequency systems, 13 MHz, the magnetic field (near-filed) is used as the RF-mechanism for power transfer between two coil antennas, while UHF, 915 MHz, use electromagnetic field (far-field) antennas. The main advantages by using magnetic coupling is the ability to monitor in difficult environments, such as on metals, in liquids, in the human body and in the ground where the propagation of electromagnetic waves is strongly limited. The UHF tags, which depend on line of sight communication, has advantages with higher data rates, communication over longer distances, and with large tag populations, as well as more compact size due to less bulky antennas.

One important factor that affects the performance of remotely powered tags is the efficiency of the rectifier block, which is located directly at the output of the antenna in the analog front end. The ability to convert a weak incoming signal to a stable power supply with enough current to support a complex chip is one of the keys in meeting future demands on RFID technology. The efficiency, in low voltage integrated circuit rectifiers, is limited not only by reverse leakage in the diodes that are used for the AC to DC conversion. The diodes also have a fixed turn on voltage that create a dead
Figure 1: I-V characteristics of MOS diodes in CMOS, including the proposed diode with full
threshold cancellation (FTC), the internal threshold cancellation diode (ITC) and the diode
connected MOS transistor (MD).

zone, where the received power is wasted as the generated voltage will be too low to
power up the tag. There are several techniques that are used to reduce the turn on
voltage, including Schottky diodes (Titanium-Silicon), low Vth transistors and dual-poly
floating gate transistors. All of these require advanced CMOS processing at an additional
cost [1] [2]. In standard CMOS, different threshold cancellation techniques have been
proposed for diode-connected MOS transistors to improve the power conversion efficiency
(PCE) of RFID rectifiers. In [3], an external Vth-cancellation technique that use the on-
chip supply voltage together with switched capacitor technique in a semi-active tag, was
introduced. The internal threshold cancellation technique (ITC) was introduced for a
passive UHF tag in CMOS [4]. In this technique the DC-output voltage of the rectifier
is used to bias the gates so that the effective threshold is reduced. Similarly, in the self
Vth-cancellation scheme (SVC) [5], the output voltage is used for improved rectification
with diode-connected MOS transistors for passive tags. Due to rapidly increased reverse
leakage at larger input voltages, the SVC technique achieves high efficiency at a single
input power level.

In this work an active MOS diode with full threshold cancellation (FTC) is proposed
that is based on the ITC technique. The proposed diode uses a control scheme to minimize
the reverse leakage that is associated with the ITC diode, while achieving full threshold
cancellation, as illustrated in Fig. 1. In section 2 of this paper, the limitations with
the internal threshold cancellation technique is theoretically analysed. Section 3 presents
the proposed diode including an short design procedure. Results from Cadence Spectre
simulations are presented in section 4, followed by the conclusions in section 5.
2. Threshold Cancellation

The internal threshold cancellation technique is illustrated in Fig. 6. The diode connected MOS transistor, M2, generates the bias voltage, \( V_b \), so that the effective threshold of the diode connected PMOS transistor M1 is reduced. Thus, the diode voltage, \( V_D \), is determined by the difference in gate bias between M1 and M2. By increasing the gate bias, \( V_b \), the effective threshold of M1 will be reduced. However if the effective threshold becomes too small, the reverse leakage of the diode will rapidly become too large, as shown below: Based on a theoretical model for ITC MOS diodes [6], the diode voltage, \( V_D \), is given as

\[
V_D \approx \sqrt{\frac{2\pi}{\beta_1} I_{out} + nU_T \ln \left( \frac{I_s}{I_b} \right)} \quad \text{where} \quad I_s > 10I_b.  
\]  

The MOS gain factor \( \beta = \mu_p C_{ox} \frac{W}{L} \), the specific current \( I_s = 2n\beta_2 U_T^2 \) \[7\] where factor \( n \), ranges from 1.2 to 1.6, and the thermal voltage, \( U_T \), is about 26 mV at room temperature. An expression for the reverse leakage\(^1\), is given by the same model as

\[
I_L \approx I_b \frac{W_1}{W_2} \approx \frac{V_{in} - V_{SG}}{R_b} \frac{W_1}{W_2} \]  

where \( I_b \) is the bias current of M2 and \( W_1, W_2 \) are the widths of M1 and M2 respectively.

Thus, according to (2) and (2), choosing the bias current larger, to reduce the diode voltage, will simultaneously increase the reverse leakage as also illustrated in Fig. 3. Clearly this will result in excessive losses in the ITC diode that degrades the power conversion efficiency. Therefore transistor M2 must be biased to operate in weak inversion so that only partial cancellation of the threshold voltage of M1 is achieved (\( V_b \leq V_{th} \)). Typically this limits rectifiers with ITC MOS diodes to a voltage drop of 200-300 mV for a power conversion efficiency above 60% as shown in section 4.

\(^1\) The effect of channel length modulation is neglected here for simplicity.
3 Proposed Diode

The main drawback with ITC MOS diodes is the reverse leakage that both limits the power conversion efficiency and prevents a low diode voltage. In order to reduce the reverse leakage, a modified ITC MOS diode is proposed in Fig. 7 for low power RFID applications [8]. In addition to the \(V_b\)-generator, M2, the proposed diode uses a CMOS inverter, M3 and M4, and a MOS diode M5. The purpose of the inverter is to turn off M1 completely during the negative half-period of the input signal, and to activate the threshold cancellation during the positive half-period as illustrated in Fig. 8. Instead of connecting the gate to the \(V_b\)-generator in the positive half-period, the gate can be connected directly to ground so that M1 operates as a controlled switch [9]. However, this can result in reverse charge leakage [8] that degrade efficiency, as M1 will be on for a short period of time in the negative half-period. In the proposed circuit, the inverter has its negative supply connected to the \(V_b\)-generator, M2, and its positive supply connected to \(V_{out}\). During the positive half-period of the input signal, the negative supply connects to the gate of M1 so that its drain-gate voltage equals \(V_b\) and the internal threshold cancellation is activated. Similarly, during the negative half-period of the input signal, the positive supply connects to the gate so that the drain-gate voltage is zero and the reverse leakage is minimised. The second MOS diode, M5, is added so that both M3 and M4 switch from on to off when \(V_{in} = V_{out}\) as shown below:

\[
V_{in} - V_{SG2} + V_{SG3} = V_{out} \rightarrow M_3 \text{ is on when } V_{in} < V_{out}
\]

\[
V_{in} - V_{GS4} + V_{SG5} = V_{out} \rightarrow M_4 \text{ is on when } V_{in} > V_{out}.
\]

One advantage of the described control scheme, except minimised leakage, is that in
3. Proposed Diode

contrast to when optimizing the ITC diode (2), the $V_b$-generator can be chosen minimum width, which vastly reduces the bias current needed for full threshold cancellation.

An abbreviated design procedure of the proposed diode is as follows:

**M1:** The size of M1 depends on the load current and is chosen large to limit the overdrive voltage, given as

$$V_{o1} \approx \sqrt{\frac{2\pi}{\beta_1}} I_{out}. \tag{3}$$

For higher operating frequency a smaller width will reduce the load capacitance of the inverter, so that the switching characteristics is improved.

**M2 and M5:** The MOS diodes M2 and M5 are chosen at minimum width to minimize the required bias current (maximise $R_{b2}$ and $R_{b5}$) so that $V_b \approx V_{SG5} \approx V_{ib}$.

**M3 and M4:** The size of the inverter depends on the gate capacitance of M1 and the transistor widths are chosen typically $W_3 \approx 2.5W_4$.

![Figure 4: The proposed MOS diode, with threshold cancellation and reverse leakage control, in a single diode rectifier.](image)

**Table 1: Component Values**

<table>
<thead>
<tr>
<th>Diode</th>
<th>$W_1$</th>
<th>$W_2$</th>
<th>$W_3$</th>
<th>$W_4$</th>
<th>$W_5$</th>
<th>$R_{b2}$</th>
<th>$R_{b5}$</th>
<th>$C_b$</th>
</tr>
</thead>
<tbody>
<tr>
<td>FTC 100kHz</td>
<td>300</td>
<td>1</td>
<td>25</td>
<td>10</td>
<td>1</td>
<td>700k</td>
<td>1M</td>
<td>-</td>
</tr>
<tr>
<td>FTC 1MHz</td>
<td>200</td>
<td>1</td>
<td>5</td>
<td>5</td>
<td>1</td>
<td>700k</td>
<td>1M</td>
<td>5p</td>
</tr>
<tr>
<td>ITC</td>
<td>200</td>
<td>2000</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>700k</td>
<td>-</td>
<td>5p</td>
</tr>
</tbody>
</table>

*(W in μm, R in Ω and C in F)*
Figure 5: Illustration of the leakage control scheme, where the current and gate voltage of M1 is plotted together with the input signal.

4 Results

The proposed FTC diode was implemented in the AMS 0.35 μm CMOS process and simulated in Cadence Spectre. Two versions were designed to verify performance both at 100 kHz and 1 MHz, and to compare with the ITC diode. Component values were chosen according to Table 1. The diodes were simulated in a single diode rectifier circuit (Fig. 7), with a sinusoidal input signal and with a large smoothing capacitor ($C_L$) and a DC-current load ($I_{out}$) connected to the output. Power and voltage conversion efficiency was simulated based on the following equations:

$$VCE = \frac{V_{out}}{\hat{V}_{in}} 100 = \frac{\hat{V}_{in} - V_D}{\hat{V}_{in}} 100 \text{ (%)}$$  \hspace{1cm} (4)

$$PCE = \frac{P_{out,DC}}{P_{in,RF}} 100 = \frac{P_{out,DC}}{P_{out,DC} + P_{loss}} 100 \text{ (%)}.$$  \hspace{1cm} (5)

The simulation results in Fig. 2 and in Fig. 3 show that the proposed FTC diode clearly improves both voltage and power conversion efficiency at all simulated input levels. The highest PCE achieved is 90 % for the FTC diode at 100 kHz at the peak voltage 1 V. Here, the VCE is 92 % and the diode voltage, $V_D$, is 80 mV. The 1 MHz design of the FTC diode has slightly lower efficiency at all input levels. This is mainly because when increasing the frequency, the inverter will generate a smaller gate pulse, $V_G$, (Fig. 8), due to limited rise and fall time, so that the threshold cancellation is reduced. As a result the PCE drops since more power is dissipated in M1 when the diode voltage, $V_D$, becomes larger. The PCE (Fig. 3) for all diodes except the MOS diode is degraded for higher input voltages. This can be explained by DC power dissipation in the $V_G$-generator, $P_b = I_b V_{out}$, that increase rapidly as both $V_{out}$ and $I_b$ increase with the input voltage. Thus, the maximas in the PCE characteristics can be displaced by varying the bias resistor of the $V_G$-generator. In the ITC diode the loss due to reverse leakage increase...
4. Results

rapidly as well with the input voltage [6]. Therefore the width \( W_2 \) is chosen ten times larger than \( W_1 \) (2), for the ITC diode, to avoid rapidly reduced efficiency for higher input voltages. The simulated power dissipation in the FTC diode at 1 MHz and 1.5 V input signal was 1 \( \mu \)W, 1.3 \( \mu \)W, 0.3 \( \mu \)W and 0.2 \( \mu \)W in M1, the \( V_b \)-generator, M5 with \( R_b \), and the inverter respectively.

Fig. 8 show the efficiency simulated for the 1 MHz FTC diode, with the design optimized for large current loads. Here a PCE above 80 % and VCE above 90 % is demonstrated for about 1 decade in variation of the load current. A maxima in PCE around 500 \( \mu \)A indicate that there is a trade-off between voltage and power conversion efficiency.
5 Conclusion

An active MOS diode based on the technique with internal threshold cancellation (ITC) in RFID rectifiers for both low and high frequency applications, is presented. The proposed diode use a control scheme that turns off the diode completely in the reverse state, and activates threshold cancellation in the forward state, so that reverse leakage is minimised and full threshold cancellation can be achieved for a wide range of input voltages and load currents. Simulated in a single diode rectifier circuit with Cadence Spectre in AMS 0.35 μm CMOS, the proposed MOS diode demonstrates an efficiency well above 80 % and 90 % for PCE and VCE respectively.

6 Acknowledgements

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A Discrete Model of the DC Charge-up Phase in RFID Rectifiers

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A Discrete Model of the DC Charge-Up Phase in RFID Rectifiers

Hans Rabén, Johan Borg and Jonny Johansson

Abstract

This paper presents a discrete model of the DC charge-up phase in a single MOS diode rectifier for an inductively coupled RFID system. The model was derived for a rectifier driven by a coil antenna and with a storage capacitor connected to the output. A comparison between the model and a simulation of a rectifier implemented in a 0.35 μm CMOS process demonstrated fast and accurate modeling of the charge up-phase for both LF and HF RFID applications. The model was used to determine the relationship between the voltage induced in the coil antenna and the available chip current based on a specification for the durations of the charge-up and the data-communication phases in a typical LF RFID application.

1 Introduction

In a typical RFID system, a passive tag is powered remotely by a radio frequency signal sent from a reader unit. The energy in the RF signal is converted to a DC-supply voltage in the analog front-end of the tag. The operation of a passive RFID tag is separated into two phases; the charge-up phase and the data transmission phase [1–3]. During the charge-up phase the reader sends a continuous RF signal to generate the DC supply voltage in the rectifier block, while the rest of the functional blocks on the tag remain in stand by mode. At the end of the charge-up phase, when the storage capacitor at the rectifier output reaches the required DC level, the chip is activated for the data transmission phase. In a simple sequence of communication between the reader and tag, where the charge-up phase is followed by data communication, the reader addresses a tag, and the tag that recognizes the address responds by sending its tag ID [4]. The time available for charge-up and data communication determines the read time for a tag, which is an important parameter of the system’s performance. For example in the low-frequency RFID standard ISO 14223, the charge-up time is 25 to 50 ms, while the command phase is typically 15 ms [5].

The specification for the charge-up time requires the rectifier block to efficiently use the incoming RF power so that the requisite level of the supply voltage can be reached. This can be particularly important for applications in the process industry where RFID technology is used to trace a process flow [6–8].

Normally in the design of rectifiers for RFID applications, the rectifier block is characterised during steady state with a constant resistive load or with a current source that
represents the power consumed by the tag [9,10]. Although this analysis can indicate the efficiency of a rectifier in terms of power and voltage conversion for comparison to other designs, it does not indicate whether a specific rectifier block will satisfy the specified requirements of the charge-up phase.

This paper presents a model of RF to DC conversion during the transient DC charge-up phase for an inductively coupled RFID system. The model is based on rectifiers using diode-connected MOS transistors and allows for accurate and fast computation of the charge-up phase for different MOS diode designs. In addition the model allows calculation of the maximum available chip current given the time required for charge-up and data communication.

The rest of this paper is organized as follows. In section 2, the model is derived. Section 3 presents the results, including model verification, a LF application example, and a comparison of the computational time between the model and simulation. Section 6 presents the conclusions of the paper.

2 Model

In this section the model is derived for the charge-up phase of the inductively coupled RFID system. First, a simple model is derived to describe the charge-up of a capacitor in a single diode rectifier with an ideal voltage source. The ideal source is then replaced with a resonance circuit to model the inductively coupled system.

2.1 Ideal voltage source

In the single diode rectifier shown in Fig. 1, a MOS diode is used for rectification. This is typical for low cost integrated RFID rectifiers [11]. The rectifier is connected to a storage capacitor $C_S$ that is chosen to be sufficiently large to supply the chip with enough current during the communication phase [12].

The peak forward current of the MOS diode [13] can be written as

$$I_D = \frac{\beta}{2}(V_D - V_i)^2$$

(1)
where $\beta$ is the MOS gain factor $\mu_F C_{ox} \frac{W}{L}$ [14] and $V_t$ is the MOS threshold voltage. An expression for the peak diode voltage can be derived based on Fig. 2, which shows the charge-up of the storage capacitor in a single diode rectifier. The diode voltage at the instant of the peak diode current can be written as

$$\hat{V}_{D_n} \approx \hat{V}_{in} - \sum_{k=1}^{n-1} V_{C_k} - \frac{V_{C_n}}{3}$$

where the middle term represents the sum of the voltage steps preceding pulse $n$ and the right term represents $1/3$ of the voltage step given by the current pulse $n$. The division of $V_{C_n}$ into two parts (Fig. 2) is based on a linear approximation of the capacitor voltage during the forward current pulse. Together with the linearization of the forward current (below) and the fact that the voltage step leads to different conduction angles when the diode turns on and off, this yields a factor less than the expected value of $1/2$. In practice, a factor of $1/3$ agrees well with the simulations.

The step size of the capacitor voltage can be written as

$$V_{C_n} = \frac{Q_n}{C} \approx \frac{I_{D_n} t}{C} \approx \frac{I_{D_n} t_n}{2C}$$

where $Q_n$ is the increase in capacitor charge, $I_{D_n}$ is the average diode current and $t_n$ is the duration of the current pulse. The average current in the above equation is derived

![Figure 2: Charge-up of the storage capacitor as a function of the number (n) of diode current pulses. The single MOS diode rectifier is simulated with a constant input voltage where each positive cycle of the input signal generates a current pulse through the diode that increases the capacitor voltage stepwise.](image)
using triangular approximation of the current pulse [15]. The time period of the current pulse can be written

\[ t_n = \frac{T}{2\pi} (\pi - 2\theta_n) \]  

(4)

where the conduction angle is given by

\[ \theta_n \approx \arcsin \left( \frac{V_{in} + \sum_{k} V_{C_k}}{V_{in}} \right). \]  

(5)

Combining (1)-(3) yields

\[ \hat{I}_D = \beta \left( \hat{V}_{in} - \frac{\sum_{k} V_{C_k}}{6C} - V_t \right)^2 \]  

(6)

Solving for \( \hat{I}_D \), and after simplifying the result by factorization, the diode peak current can be written as

\[ \hat{I}_{Dn} \approx a_n \left( b_n + \frac{a_n}{\beta} \right) \]  

(7)

where the factors \( a_n \) and \( b_n \) are given as

\[ a_n = \frac{6C}{t_n} \]  

(8)

and

\[ b_n = \hat{V}_{in} - V_t - \sum_{k} V_{C_k}. \]  

(9)

By summing the voltage steps given by (3) for the number of pulses \( n \), the total capacitor voltage can be written as

\[ V_C = \sum_{k} V_{C_k} \approx \frac{\hat{I}_{Dk} t_k}{2C} \]  

(10)

where \( \hat{I}_{Dk} \) and \( t_k \) are given by (7) and (4) respectively. To express \( V_{C_k} \) as a function of time, \( n \) is multiplied by the time period \( T \) of the sinusoidal input voltage.

2.2 Resonance circuit

Fig. 3 shows an inductively coupled RFID reader antenna and a tag coil antenna with a resonance circuit \((L_1, R_1, C_1)\). The resonance circuit increases the amplitude of the weak input signal \( u_i \) that is induced in the tag coil antenna by the continuous RF signal sent from the reader, before RF to DC conversion is achieved in the rectifier block.

To introduce the tag coil antenna into the derived model, the ideal voltage source \( V_{in} \) in Fig. 1 is replaced by the tag coil antenna, connecting the output of the resonance circuit to the input of the single diode rectifier.

The relationship between the induced voltage and the input voltage of the rectifier is given at resonance by

\[ \hat{V}_{in} = Q_L \hat{u}_i. \]  

(11)
Figure 3: Equivalent circuit of inductively coupled coil antennas in an RFID system. The induced voltage is given by $u_i = j\omega M_i q_2$, where $M$ is the mutual inductance of the two antennas [16].

$Q_L$ is the loaded quality factor of the resonance circuit with the resistive load $R_{IN}$, represented here by the input resistance of the rectifier [16]. The quality factor is written as

$$Q_L = \frac{1}{Q_1 + \frac{X_1}{R_{IN}}}$$

(12)

where the quality factor of the unloaded coil is $Q_1 = X_1/R_1 = \omega L_1/R_1$.

Due to the pulsed characteristic of the input current of the rectifier together with the continuous sinusoidal input voltage generated by the resonance circuit, the input resistance is strongly nonlinear. However, to introduce the rectifier input resistance into (12) so that the circuit can be properly modeled, an average input resistance can be derived [17].

The average input voltage and average input current during one period with a sinusoidal input voltage (Fig. 2) are given by

$$\bar{V}_{in} = \frac{V_{in}}{\pi}$$

(13)

and

$$\bar{I}_{in} = t_n I_{D_n} \frac{2}{T}$$

(14)

so that the average input resistance becomes

$$\bar{R}_{in} = \frac{\bar{V}_{in}}{\bar{I}_{in}} \approx \frac{2V_{in}T}{\pi t_n I_{D_n}}$$

(15)

Combining (15), (12) and (11) yields

$$\hat{V}_{in} = \frac{1}{Q_1} \left( \hat{u}_i + \frac{X_1 \pi t_n I_{D_n}}{2V_{in}T} \right)$$

(16)

Solving for $\hat{V}_{in}$ gives the peak input voltage as

$$\hat{V}_{in} \approx Q_1 \left( \hat{u}_i + \frac{X_1 \pi t_n I_{D_n}}{2T} \right).$$

(17)
The conduction angle is derived from (17), (5) and (4), which after simplifications can be written as

$$\theta_n \approx \arcsin\left( \frac{V_i + \sum_{k=1}^{n-1} V_{C_k}}{Q_1 \hat{u}_i} \right).$$  \hspace{1cm} (18)

Substituting (17) into (2) to recalculate the diode peak current yields the capacitor voltage from equations (10) and (7), as before, but with the conduction angle from (18) and new coefficients for $a_n$ and $b_n$ written as

$$a_n = \frac{3}{t_n \left( \frac{Q_1 \hat{u}_i}{2} + \frac{1}{2n} \right)}$$  \hspace{1cm} (19)

and

$$b_n = Q_1 \hat{u}_i - V_i - \sum_{k=1}^{n-1} V_{C_k}.$$  \hspace{1cm} (20)

### 3 Results

In this section, the model is verified for a single diode rectifier driven with an HF coil antenna, followed by an LF application example and a comparison of computational time between model and simulation.

![Figure 4: Model verification for a single diode rectifier with a resonance input circuit at f=13 MHz. The variables on the traces are from left to right $u_i$, $C_S$ and the width $W$ of the MOS diode, which is 30 μm for unmarked traces.](image-url)
Figure 5: Modeling the single diode rectifier with a resonance input circuit at $f=13$ MHz with different weighting factors for the model parameters $a_n$ and $\theta_n$. The value of the storage capacitor is $C_S=20$ nF, and $u_i$ is 130 mV and 75 mV for the upper and lower set of traces, respectively.

3.1 Model Verification

To verify the derived model of the inductively coupled system, a single MOS diode rectifier was simulated in a 0.35 $\mu$m CMOS process together with a resonance circuit (Fig. 3). The resonance circuit was designed to resonate at 13 MHz with an HF coil antenna [16] with an inductance of $L_1=0.5$ $\mu$H, an internal resistance of $R_1=1$ $\Omega$ and with $C_1=276$ pF. The process parameters of the pMOS diode used in the simulations were introduced in the model to calculate the MOS gain factor $\beta$ (1). The derived model was implemented in MATLAB based on (4),(7) and (18)-(20).

A comparison based on Fig. 4 shows good agreement between the model and the simulation, with the model slightly underestimating $V_C$ for the larger transistor width. This deviation can be partly explained by the subthreshold current [18] in the simulation of a MOS diode, which increases the DC output voltage of this circuit. This effect, which becomes more pronounced when the width of the MOS diode is increased, is not included in the model. Fig. 4 also shows the charge-up using a MOS diode with the same $\beta$ but $V_t=0.25$ V, which is used here to mimic the characteristics of a typical Schottky diode.

Fig. 5 presents an illustration of how different parameters of the model affect the charge-up phase. The plots show that the factor $a_n$ (19) and the conduction angle $\theta_n$ (18) can be calibrated to fit the model to a simulation, which may be necessary as the model starts to deviate for rapid charging of small capacitors. However, in most cases relevant
for RFID applications, the best fit is achieved without changing these parameters.

### 3.2 LF application example

As an example application, the model is used here to determine the relationship between the voltage induced in the coil antenna and the available chip current from the rectifier output for a typical LF application with a ferrite stick antenna [5].

As briefly discussed in Section 2.1, the chip current is supplied from the storage capacitor, which is used as a voltage source during the data communication phase to send a reply to the reader. The current consumption of the chip can be introduced into the derived model by the following relationship, where the size of the storage capacitor $C_S$ that can supply the chip with the current $I_{\text{Chip}}$ during the time $t_2$ is given by

$$C_S = \frac{Q}{U} = \frac{I_{\text{Chip}}t_2}{V_{\text{max}} - V_{\text{min}}}$$

(21)

![Figure 6: The charge-up phase of the storage capacitor of a rectifier with a resonance input circuit at f=134.2 kHz for three different values of $u_i$. Normally, a voltage limiter is used to prevent the supply voltage from exceeding $V_{\text{max}}$.](image)
3. Results

where $V_{\text{max}}$ and $V_{\text{min}}$ are the upper and lower limits of the chip supply voltage that allows for proper tag operation during the data communication phase [16].

Given the above equation, the coil voltage $u_i$ that is needed to generate the charge $Q$ that can supply the chip current $I_{\text{Chip}}$ was determined as follows: After calculating $C_S$ from (21) for a given chip current $I_{\text{Chip}}$, the charge-up of $C_S$ was plotted for different values of the coil voltage $u_i$. An example, based on the values in Table 1, where the coil voltage required to charge $C_S$ to $V_{\text{max}}$ within the time $t_1$, was determined to 183 mV as shown in Fig. 6. The capacitor $C_S$ in the example was calculated for $I_{\text{Chip}}=25 \mu A$, and the model was implemented based on (4),(7) and (18)-(20).

The method described above was used to model the relationship between the induced voltage and the available chip current, as shown in Fig. 7. The chip current is plotted as a function of the coil voltage in the range of 130-270 mV, where the lower voltage limit represents the minimum induced voltage that can generate the required supply voltage with a single diode rectifier. The minimum coil voltage was calculated as

$$u_i \approx \frac{V_{\text{max}} + V_t}{Q_1} \approx 130mV. \tag{22}$$

Increasing $u_i$ from the minimum voltage reveals the relationship between $u_i$ and $I_{\text{Chip}}$ for this LF application.
Table 2: Comparison of computational time

<table>
<thead>
<tr>
<th>Application</th>
<th>Model</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>LF : $f=134.2$ kHz and $t=50$ mS</td>
<td>0.07 s</td>
<td>1 min 45 s</td>
</tr>
<tr>
<td>HF : $f=13.56$ MHz and $t=10$ mS</td>
<td>1.11 s</td>
<td>23 min 16 s</td>
</tr>
</tbody>
</table>

3.3 Computational time

The computation time required to plot the charge-up phase is compared between the model and the simulation for both LF and HF applications. The computations for the model are implemented in MATLAB, while the simulations are performed using Cadence Spectre with transient analysis. As shown in Table 2, the MATLAB-based model for rectifiers can drastically reduce the computational time, which quickly becomes problematic for the simulations, as the frequency increases when transient analysis is used for rectifier design and evaluation.

4 Conclusion

This paper presented a model of the DC charge-up phase in rectifiers for inductive RFID applications. The model achieved fast and accurate modeling of the RF to DC conversion with different MOS diodes for both LF and HF applications. A rectifier was also modeled to illustrate how the available chip current depends on the induced antenna voltage, given a specified time for charge-up and data communication. The simplicity of the model presented here for a single diode rectifier allows for the modeling of larger diode-based architectures such as multi-stage rectifiers for low-voltage applications.

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References


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Design of Voltage Multipliers for Maximized DC Generation in Inductively Coupled RFID Tags

Hans Rabén, Johan Borg and Jonny Johansson

Abstract

This paper presents models, circuit solutions and design procedures for maximized DC generation in inductively coupled RFID tags. An analytical model for the DC generation is derived, and relationships between the received signal in the tag coil antenna and the generated DC supply voltage using a voltage multiplier, based on both passive and active diodes, are presented. Derived from the trade-off between voltage gain in the multiplier and the tag coil at resonance, an equation for the optimum number of multiplier stages to achieve maximized DC generation is presented. Based on the derived equation, design examples are included with two typical tag coil antennas given a specification of the DC supply voltage and current. Also included in this paper is the design of a voltage multiplier based on active diodes implemented and manufactured in AMS 0.35 μm CMOS process. The active diodes are based on a concept of threshold cancellation of MOS diodes and make use of reverse leakage control to achieve full threshold cancellation.

1 Introduction

In an inductively coupled RFID system efficient use of the power transmitted from a remote reader to power the battery-less chip in a passive tag is one of the keys to meeting future demands, such as improved readability in harsh environments, higher security as well as reduced cost per tag [1].

To generate the DC supply voltage for an inductive RFID tag, a continuous signal is sent by the reader to power the passive tag, as shown in Fig. 1. The coil antenna in the tag front end captures the signal, and after voltage gain in a resonance circuit, the signal is converted to a DC supply voltage in the rectifier block. To maximize the voltage gain in the rectifier block, a multi-stage rectifier, also called a voltage multiplier, is commonly used. In the resonance circuit, the voltage gain is favored by a high input resistance of the rectifier block [2]. However, when increasing the number of stages to maximize the voltage gain in the rectifier block, the input resistance is reduced [3]. Thus, the combination of a resonance circuit with a voltage multiplier results in a trade-off between voltage gain in the resonance circuit and in the voltage multiplier. Although several analytical models

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Figure 1: DC generation for an inductively coupled RFID tag. The signal received by the coil antenna is converted to \( V_{dc} \) by a voltage multiplier with an optimum number of stages \( N_{opt} \) (15).

have been presented for RF to DC conversion for UHF RFID [3–5], no analytical models have been presented for inductive RFID that include the resonance circuit in the analysis.

A second important factor that affects the DC generation for an RFID tag is the conversion efficiency of the rectifier block. The voltage and power conversion efficiency of the rectifier are defined as \( VCE = \frac{V_{out}}{V_{in}} \) and \( PCE = \frac{P_{out}}{P_{in}} \), respectively. Increasing the PCE by reducing the required input power to the rectifier block, or equivalently increasing the input resistance, favors voltage gain in the resonance circuit, as discussed above.

Furthermore, the conversion efficiency in integrated circuit rectifiers is limited mainly by the diode voltage of the diodes used in the AC to DC conversion. The voltage drop across the diodes in the rectifier block results not only in reduced VCE but also in reduced PCE, as the forward current creates power dissipation in the diodes. Several techniques have been proposed to reduce the diode voltage in integrated rectifiers for RFID applications. In addition to techniques that require advanced and costly semiconductor processing, such as inclusion of Schottky diodes, low \( V_{th} \) and floating gate transistors [6, 7], several threshold cancellation techniques have been proposed for diode connected transistors in standard CMOS [8–10]. Active diodes have also been proposed for CMOS-based comparator driven switches for RFID applications in the mW range [11, 12].

This paper presents analytical models, circuit solutions and design procedures that allow maximized DC generation in inductive RFID tags. An analytical model for the DC generation in inductive tags using a voltage multiplier based on both passive and active diodes is derived. Relationships between the received signal and the generated DC voltage are presented as well as an equation for the optimum number of stages to achieve maximized DC generation (Fig. 1). This paper also includes the design of a voltage multiplier in CMOS based on the active diode proposed in [13]. The diode is based on a technique with threshold cancellation and is modified here for reduced power consumption in the multiplier architecture. The designed voltage multiplier is simulated with a resonance circuit in Cadence Spectre, for verification of the DC generation model for multipliers based on active diodes and for comparison to related work. To verify performance, the proposed multiplier is implemented and manufactured in AMS 0.35 \( \mu m \) CMOS process.

In section 2 of this paper, the analytical model for the DC generation is derived and verified with Cadence simulations. The section includes design examples of multipliers
for maximized DC generation using typical coil antennas at the frequencies 125 kHz and 13 MHz. The design examples also include a comparison for how the DC generation affect the distance to the reader. Section 3 briefly presents the technique with threshold cancellation of MOS diodes, followed by a detailed presentation of the proposed active diode, including a short design procedure. The design of the proposed voltage multiplier in CMOS is presented in Section 4, while the implementation and the measurement results are presented in Section 5. Finally the paper is concluded in Section 6.

2 Modelling The N-stage Voltage Multiplier

The following subsections present an analytical model for DC generation using a voltage multiplier based on both passive and active diodes. Relationships between the input signal and the generated DC voltage are derived for the voltage multiplier, driven both by a voltage source with an output resistance and by a resonance circuit. An equation is derived for the optimum number of stages to achieve maximized DC generation. Based on this result, design examples given a specified coil antenna and a DC supply voltage and current are presented.

2.1 Passive diodes

The derivation of the voltage and power conversion efficiency is briefly summarized below for $N$-stage multipliers based on passive diodes and with an output load current $I_{dc}$, as described in [14].

For the voltage multiplier in Fig. 2 the output voltage is written as

$$V_{dc} = 2N(\hat{v}_{ac} - V_d)$$

where $V_d$ is the diode voltage. The voltage conversion efficiency is written as

$$VCE = \frac{V_{dc}}{2N\hat{v}_{ac}} \times 100 = \frac{V_{dc}}{V_{dc} + 2NV_d} \times 100(\%)$$

(2)

The power conversion efficiency is defined as

$$PCE = \frac{P_{out}}{P_{in}} \times 100 = \frac{P_{out}}{P_{out} + P_{loss}} \times 100(\%)$$

(3)

where the output power is written as

$$P_{out} = V_{dc}I_{dc}.$$  

(4)

The power dissipation in the diodes due to forward current is written as

$$P_{loss} = 2NV_dI_{dc}.$$  

(5)

so that the power conversion efficiency becomes
Figure 2: N-stage voltage multiplier based on the Greinacher voltage doubler marked in the figure.

\[ PCE = \frac{V_{dc}I_{dc}}{V_{dc}I_{dc} + 2NV_dI_{dc}} = \frac{V_{dc}}{V_{dc} + 2NV_d}, \]  

(6)

It is apparent from the above equation that aside from the expressions for the voltage and power conversion being equal, the efficiency is degraded by increasing N. However, it will be shown below that when driven with the voltage source or the resonance circuit, adding more stages can still improve the conversion efficiency.

For a voltage source \( V_s \) with an output resistance \( R_s \) connected to the input of the voltage multiplier in Fig. 2, a relationship between the source peak voltage \( \hat{v}_s \) and the multiplier peak input voltage \( \hat{v}_{ac} \) can be derived. Voltage division between the input resistance \( R_{in} \) of the voltage multiplier and the source resistance \( R_s \) yields

\[ \hat{v}_{ac} = \hat{v}_s \left( \frac{R_{in}}{R_{in} + R_s} \right). \]  

(7)

Due to the pulsed characteristic of the input current of the rectifier, together with a continuous sinusoidal input voltage, the input resistance is strongly nonlinear. However, an equivalent input resistance [14] can be derived as

\[ R_{in} \approx R_{eq} = \frac{\hat{v}_{ac}^2}{2P_{in}} = \frac{\hat{v}_{ac}^2}{2(P_{out} + P_{loss})}. \]  

(8)

Combining (1),(7) and (8) yields the required source voltage for a targeted output \( V_{dc} \) as

\[ \hat{v}_s = \frac{V_{dc}}{2N} + V_d + 4NI_{dc}R_s. \]  

(9)

By analyzing the above equation, it is clear that for the case when the supply current \( I_{dc} > 0 \), a local minimum exists for \( \hat{v}_s \) as function of \( N \). Thus, an expression for the optimum value of \( N \) can be derived: Solving \( \partial\hat{v}_s/\partial N = 0 \) for \( N \) yields
2. Modelling The $N$-stage Voltage Multiplier

Figure 3: Equivalent circuit for inductively coupled coil antennas in an RFID system. The induced antenna voltage is given by $u_i = j \omega i_2 k \sqrt{L_1 L_2}$, where $k$ is the coupling coefficient of two parallel antennas centered on the same axis [2].

$$N_{\text{opt}} = \sqrt{\frac{V_{\text{dc}}}{8 I_{\text{dc}} R_s}} = \frac{1}{2 \sqrt{2}} \sqrt{\frac{R_L}{R_s}}.$$  \hspace{1cm} (10)

Substituting (10) in (9) gives the relationship between the required source voltage and the targeted output voltage $V_{\text{dc}}$ and the current $I_{\text{dc}}$ as

$$\hat{v}_s = \sqrt{8 V_{\text{dc}} I_{\text{dc}} R_s} + V_d.$$  \hspace{1cm} (11)

Based on this result, it can also be shown that for a voltage multiplier with $N_{\text{opt}}$ stages, the input resistance $R_{eq}$ of the multiplier equals $R_s$ as the diode voltage $V_d$ goes to zero, so that maximum power transfer is achieved from the source to the load. This conclusion that maximum DC generation is achieved at power match, also explains the existence of $N_{\text{opt}}$: When increasing $N$ the input resistance of the multiplier is initially reduced towards $R_s$ while further increasing $N$ will create mismatch as the input resistance reduces below $R_s$.

2.2 Resonance circuit

Fig. 3 shows an inductively coupled RFID reader antenna and a tag coil antenna with a resonance circuit $(L_1, R_1, C_1)$. The resonance circuit increases the amplitude of the weak input signal $u_i$ that is induced in the tag coil antenna by the continuous signal sent from the reader, before DC generation is achieved in the rectifier block.

To introduce the coil antenna as the source driving the voltage multiplier, a Thevenin equivalent is derived. As shown in Fig. 4, the inductor $L_1$ with the internal resistance $R_1$ is transformed from a series to a parallel network [15], which at resonance simplifies to a Thevenin equivalent where $\hat{v}_s$ and $R_s$ are written as

$$\hat{v}_s = \hat{u}_i Q_1$$  \hspace{1cm} (12)

and

$$R_s = R_1 Q_1^2.$$  \hspace{1cm} (13)

Substituting the equations for the derived Thevenin equivalent of the resonance circuit (12) and (13) into (9) yields
\[ \dot{u}_i = \frac{1}{Q_1} \left( \frac{V_{dc}}{2N} + V_d \right) + 4N X_1 I_{dc} \tag{14} \]

where \( X_1 \) is the absolute value of the reactance of the coil antenna given by \( X_1 = \omega L_1 \).

The optimal number of stages of the voltage multiplier when driven with a coil antenna is given by substituting (13) in (10) as

\[ N_{opt} = \frac{1}{2\sqrt{2Q_1}} \sqrt{\frac{R_i}{R_i}} = \frac{1}{2\sqrt{2Q_1}} \sqrt{\frac{V_{dc}}{I_{dc}R_i}} \tag{15} \]

and the required coil voltage is given by (11)-(13) as

\[ \dot{u}_i = \sqrt{8V_{dc}I_{dc}R_i} + \frac{V_d}{Q_1} \tag{16} \]

The derived analytical model was verified with circuit simulation of the voltage multiplier, as shown in Fig. 5. In addition to good agreement between model and simulation, the simulation confirms that the maximum voltage conversion occurs at \( N_{opt} \) despite reduced efficiency in the rectifier. The result is also a confirmation that the introduction of an equivalent input resistance (8) of the rectifier serves well as an approximation in the derivation of the model.

### 2.3 Design example for Maximized DC generation

Based on the derived model for the voltage multiplier driven by a resonant circuit, a short design procedure can be outlined. As shown above, the procedure allows maximized DC generation by minimizing the induced coil voltage that is required to meet the target output voltage and current. Given a tag coil antenna with the inductance \( L_1 \) and the internal resistance \( R_1 \) as well as a specified chip voltage \( V_{dc} \) and current \( I_{dc} \):

1) the number of stages \( N_{opt} \) is calculated from (15), and
2) the required coil voltage \( \dot{u}_i \) is calculated from (16), where \( V_d \) is the diode voltage.

![Figure 4: a) The tag coil antenna with the resonance circuit connected to the voltage multiplier input. \( R_{eq} \) denotes the equivalent input resistance as derived in equation (8) above. b) Series to parallel transformation of the coil antenna with the condition that \( \omega = \omega_0 \approx 1/\sqrt{L_1C_1} \) and \( Q_1 >> 1 \). c) The Thevenin equivalent circuit at the resonance frequency \( \omega_0 \).](image-url)
Figure 5: Cadence simulations and analytical model (14) of the required coil voltage for the targeted $V_{dc} = 3.5 \, \text{V}$ as a function of $N$ for the voltage multiplier based on passive diodes and driven with a resonance circuit. A sinusoidal voltage at $f_0 = 125 \, \text{kHz}$ was simulated with $L_1 = 250 \, \mu\text{H}$, $R_1 = 3.9 \, \Omega$, $C_1 = 6.5 \, \text{nF}$ and MOS diodes with $V_d \approx 0.7 \, \text{V}$. $N = 0.5$ represents a single diode rectifier. Also shown in the figure is the conversion efficiency of the rectifier based on (2) and (6), as well as the theoretical values of $N_{opt}$ based on (15) marked on the $x$-axis with $X$. Note that in practice $N_{opt}$ can only be an integer or half-integer.

A summary of design examples where two different coils are used to generate a supply voltage of $V_{dc} = 3.5 \, \text{V}$ is shown in Table 1. Typical coil antennas for inductive RFID are chosen for 125 kHz and 13 MHz with Q-factors of 50 and 20 respectively, based on [2]. The optimum number of stages and the required coil voltages are calculated for both coils at two different current loads for multipliers based on passive diodes with $V_d = 0.7 \, \text{V}$. The required coil voltage $\hat{u}_{i_{d,1}}$ for DC generation with a single diode based on (14) is included for comparison. To also include a comparison for how the different required coil voltages affects the distance to the reader coil [2], an equation for the distance $x$ was derived from

$$\hat{u}_i = \omega i_2 k \sqrt{L_1 L_2}, \quad (17)$$
where \( L_1 \) and \( i_2 \) are the inductance and peak current of the reader coil as also shown in Fig. 3. The coupling coefficient \( k \) between the two coils is given by

\[
k \approx \left( \frac{r_1 r_2}{x^2 + r_2^2} \right)^{3/2} \text{ for } r_2 \geq r_1,
\]

where \( r_1 \) and \( r_2 \) are the radii’s of the tag and reader coils respectively. Substituting (18) into (17) and solving for \( x \) yields

\[
x \approx \sqrt{r_1 r_2} \left( L_1 L_2 \right)^{1/6} \left( \frac{\omega i_2}{u_i} \right)^{1/3} \text{ for } x \gg r_2.
\]

The derived equation was used to evaluate how the required coil voltage affect the distance for multipliers compared to single diodes based on

\[
\frac{x}{x_{\text{a,s}}} = \left( \frac{\hat{u}_{i_{\text{a,s}}}}{\hat{u}_{i}} \right)^{1/3}.
\]

The result in Table 1 show for example that compared to using single diodes with the load current \( I_{\text{dc}} = 15 \mu A \), a multiplier with \( N_{\text{opt}} = 4.2 \) at 13 MHz increase the distance 1.4 times while a multiplier with \( N_{\text{opt}} = 0.9 \) at 125 kHz increase the distance 1.04 times, for this choice of coil antennas. It should be noted that for RFID applications, the number of multiplier stages may be limited due to increased charge-up time of the DC output voltage, which increase with the number of capacitors in multiplier architectures [16].

### 2.4 Active diodes

Active diodes, such as MOS diodes with threshold cancellation, use auxiliary circuits to reduce the diode voltage of the MOS diode. The auxiliary circuits of the diode are powered by the input signal to make it suitable for use in rectifiers for passive RFID applications. While a reduced diode voltage results in improved voltage conversion efficiency, the main limitation with active diodes is the additional power dissipation in the auxiliary circuits that reduces the power conversion efficiency.

#### Table 1: Voltage Multiplier Design Examples

<table>
<thead>
<tr>
<th>Frequency</th>
<th>( L_1 ) (nH)</th>
<th>( R_1 ) (Ω)</th>
<th>( I_{\text{dc}} ) (μA)</th>
<th>( N_{\text{opt}} )</th>
<th>( \hat{u}_{i} ) (mV)</th>
<th>( \hat{u}<em>{i</em>{\text{a,s}}} ) (mV)</th>
<th>( x/x_{\text{a,s}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1.25 \times 10^5 )</td>
<td>15.7</td>
<td>5</td>
<td>1.5</td>
<td>61</td>
<td>92</td>
<td>1.15</td>
<td></td>
</tr>
<tr>
<td>( 1.3 \times 10^6 )</td>
<td>10^{-3}</td>
<td>15</td>
<td>0.9</td>
<td>95</td>
<td>108</td>
<td>1.04</td>
<td></td>
</tr>
<tr>
<td>( 1.5 \times 10^6 )</td>
<td>10^{-3}</td>
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<td>1.5</td>
</tr>
<tr>
<td>( 1.5 \times 10^6 )</td>
<td>10^{-6}</td>
<td>15</td>
<td>4.2</td>
<td>76</td>
<td>212</td>
<td>1.4</td>
<td></td>
</tr>
</tbody>
</table>
The derivation of a model for a voltage multiplier with active diodes is briefly presented because it follows the same procedure as for the passive diodes. While the equation for voltage conversion efficiency becomes the same as for passive diodes, given by (2), the equation for power conversion efficiency needs to account for the additional power dissipation that occurs in a rectifier based on active diodes. Given the additional power dissipation in the auxiliary circuits of one active diode, $P_{aux}$, the loss in the voltage multiplier can be written as

$$P_{loss} = 2N(V_{dc}I_{dc} + P_{aux}(V_{dc1})). \quad (21)$$

Modelling $P_{aux}$ as a function of the output voltage $V_{dc1}$ of the unit cell (Fig. 2) applies to active diodes in general, as they are commonly biased with DC current from the output.

Given the loss in the multiplier $P_{loss}$, the source voltage $\hat{v}_s$ and the antenna voltage $\hat{u}_i$, we can derive

$$PCE = \frac{V_{dc}I_{dc}}{I_{dc}(V_{dc} + 2NV_d) + 2NP_{aux}(V_{dc1})}. \quad (22)$$

$$\hat{v}_s = \frac{V_{dc}}{2N} + V_d + 4NR_s(I_{dc} + \frac{2NP_{aux}(V_{dc1})}{V_{dc} + 2NV_d}). \quad (23)$$

and

$$\hat{u}_i = \frac{1}{Q_1} \left( \frac{V_{dc}}{2N} + V_d \right) + 4NX_1(I_{dc} + \frac{2NP_{aux}(V_{dc1})}{V_{dc} + 2NV_d}). \quad (24)$$

Comparing the resulting equation for the antenna voltage using active diodes with the corresponding equation for passive diodes (14) shows that a third term is added to (24) that includes $P_{aux}$. Clearly, for $P_{aux} = 0$, equation (24) simplifies to (14). When comparing the equations for the case when $I_{dc} = 0$, a term including the reactance of the coil antenna $X_1$ remains for (24) due to the power dissipation of the active diodes. Thus, in contrast to using passive diodes for DC generation without an output load, the required coil voltage increases when a large coil inductance $L_1$ is used together with active diodes. At the same time, the required coil voltage for DC generation with active
diodes is normally favored by a lower diode voltage. The impact of the coil antenna on the DC generation with active diodes is further studied in Section 4.2.

3 The Active Diode in CMOS

In this section we present the design of an active MOS diode with full threshold cancellation (FTC) [13]. The proposed diode is based on a technique with internal threshold cancellation of diode connected MOS transistors. A brief presentation of internal threshold cancellation is followed by a detailed functional description of the proposed FTC diode as well as a short design procedure.

3.1 Threshold Cancellation

The concept of internal threshold cancellation technique (ITC) [9] is illustrated in Fig. 6. The diode connected MOS transistor, M2, generates the bias voltage, $V_b$, so that the effective threshold of the diode connected pMOS transistor M1 is reduced. Thus, the diode voltage, $V_d$, is determined by the difference in gate bias between M1 and M2. By increasing the gate bias, $V_b$, the effective threshold of M1 is reduced to minimize the diode voltage. However, as described in [13], reducing the diode voltage simultaneously increases the reverse leakage, which in turn results in reduced power conversion efficiency of the diode. This effect typically limits rectifiers with ITC MOS diodes to a voltage drop of 200-300 mV for a power conversion efficiency above 60 %, as shown in Section

![Figure 7: The proposed MOS diode, with full threshold cancellation (FTC) and reverse leakage control, in a single diode rectifier. The auxiliary circuit of the active diode is marked in the figure. For all pMOS transistors the n-well body is connected to the highest potential $V_{dc}$ of the circuit to avoid reverse substrate leakage [17].](image-url)
Figure 8: Illustration of the leakage control scheme, where the current and gate voltage of M1 is plotted together with a 100 kHz sinusoidal input signal. While no reverse leakage current is seen in the figure, a calculation showed that the forward charge for $I_{ac}$ is approximately 150 times larger than reverse charge.

3.2 The Proposed Full Threshold Cancellation Diode

To overcome the limitations with increased leakage discussed above, a full threshold cancellation (FTC) diode is proposed in Fig. 7. In addition to the $V_b$-generator, M2, the proposed diode uses a CMOS inverter, M3 and M4, a MOS diode M5, and a switch M11. The purpose of the inverter is to turn M1 completely off during the negative half-period of the input signal and to activate threshold cancellation during the positive half-period, as illustrated in Fig. 8. In the proposed circuit the inverter has its negative supply connected to the $V_b$-generator, M2, and its positive supply connected to $V_{dc}$. During the positive half-period of the input signal, the negative supply connects to the gate of M1 so that its drain-gate voltage equals $V_b$ and the threshold cancellation is activated. During the negative half-period of the input signal, the positive supply connects to the gate so that the drain-gate voltage is zero and the reverse leakage is minimized. As an alternative to the described scheme the inverter may be used to switch the gate of M1 between the positive supply and ground instead of to a $V_b$-generator so that M1 operates as a controlled switch [18]. However, this can result in reverse charge leakage that degrades efficiency, as M1 is on for a short period of time in the negative half-period, as further discussed in [19]. In the proposed scheme the inverter also drives the switch M11, which is used to turn off the bias current of the $V_b$-generator when the threshold elimination is deactivated so that power consumption can be reduced. As the switch M11 is driven in parallel with M1 by the pulse $V_g$, the duration of the bias current is effectively limited to the on-state of M1.

The second MOS diode, M5, is added so that both M3 and M4 switch from on to off
Figure 9: The unit cell of the CMOS voltage multiplier based on two active diodes. M2, M5 and M9, M10 are diode connected pMOS and nMOS transistors, respectively.

when \( \dot{v}_{ac} = V_{dc} \), as shown below:

M3 is on when \( \dot{v}_{ac} < V_{dc} \rightarrow \dot{v}_{ac} - V_{sg5} + V_{sg3} = V_{dc} \)

M4 is on when \( \dot{v}_{ac} > V_{dc} \rightarrow \dot{v}_{ac} - V_{gs4} + V_{sg2} = V_{dc} \).

One advantage of the described control scheme, apart from minimized leakage and switched bias current, is that in contrast to when an ITC diode is optimized [20], the transistor M2 of the \( V_b \)-generator can be chosen to be of minimum width, which vastly reduces the bias current needed for full threshold cancellation of the proposed MOS diode.

An abbreviated design procedure for the FTC diode is as follows:

**M1:** The size of M1 depends on the load current and is chosen to be large to limit the overdrive voltage, given as

<table>
<thead>
<tr>
<th>Component values active pMOS and nMOS diodes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>pMOS</strong></td>
</tr>
<tr>
<td>FTC</td>
</tr>
<tr>
<td>ITC</td>
</tr>
<tr>
<td><strong>nMOS</strong></td>
</tr>
<tr>
<td>FTC</td>
</tr>
<tr>
<td>ITC</td>
</tr>
</tbody>
</table>
3. The Active Diode in CMOS

Figure 10: The power dissipation in the auxiliary circuits of one active diode in the unit cell voltage doubler (Fig. 9). $P_{\text{aux}}$ was determined as the input power of the unit cell when simulated in the steady state with a sinusoidal input voltage and without output load. The two traces sw-bias and dc-bias represent simulations with and without the switches M11 and M12, respectively.

For higher operating frequency, a smaller width reduces the load capacitance of the inverter, so that the switching loss is limited. To account for this effect when sizing M1, the average power dissipation due to charging and discharging of the capacitive load $C_L$ of the inverter is written

$$V_{o1} \approx \sqrt{\frac{2\pi}{\beta_1} I_{dc}}.$$  

(25)

For higher operating frequency, a smaller width reduces the load capacitance of the inverter, so that the switching loss is limited. To account for this effect when sizing M1, the average power dissipation due to charging and discharging of the capacitive load $C_L$ of the inverter is written

$$P_{\text{avg}} = V_{dc}I_{\text{avg}} = V_{dc}fQ_{cL} \approx V_{dc}fV_L C_L.$$  

(26)

The capacitance $C_L$ is written

$$C_L \approx C_{gsM1} + C_{gsM11} \approx C_{ox}L(\frac{2}{3}W_{M1} + \frac{1}{2}W_{M11}),$$  

(27)

where the gate to source capacitances $C_{gsM1}$ and $C_{gsM11}$ are derived for M1 and M11 when operating in saturation and linear regions respectively [15]. Given the above equations the total width of M1 and M11 should be limited so that

$$P_{\text{avg}} \ll P_{\text{out}}.$$  

(28)

As an example, a total width of 350 $\mu$m and a 0.35 $\mu$m CMOS process at $V_{dc}$ 3.5 V yields an average power dissipation $P_{\text{avg}}$ of approximately 1 $\mu$W at the upper frequency limit 1 MHz [13].

**M2 and M5:** The size of the MOS diodes M2 and M5 are chosen to minimize the required bias current (maximise $R_{b2}$ and $R_{b4}$) so that $V_b \approx V_{gs} \approx V_{th}$.

**M3 and M4:** The size of the inverter depends on the gate capacitance of M1, and the transistor widths are typically chosen $W_3 \approx 2.5W_4$. 

$$V_{o1} \approx \sqrt{\frac{2\pi}{\beta_1} I_{dc}}.$$  

(25)
M11: The width of the pMOS switch M11 is chosen so that the voltage drop due to the on-resistance is negligible compared to $V_h$.

4 Proposed CMOS Voltage Multiplier

The FTC diode presented above is used in this section in the design of a voltage multiplier in 0.35 $\mu$m CMOS. A brief presentation of the design is followed by a simulation of the CMOS multiplier with a resonance circuit. The simulation results are compared to the analytical model derived in Section 2.4 for multipliers based on active diodes. Also included is a comparison of the performance for the proposed multiplier, with multipliers based on passive and ITC diodes.

4.1 Design

The multiplier architecture is based on $N$ unit cells, as shown in Fig. 2. The unit cell of the proposed CMOS voltage multiplier is based on two active diodes, M1 and M6, including auxiliary circuits, as shown in Fig. 9. The active diode M6 is designed as an nMOS version of the proposed pMOS diode M1 because a voltage doubler based on diodes with threshold cancellation requires one nMOS and one pMOS diode [9]. The component values for both diodes, based on the design procedure in Section 3.2, are presented in Table 2. All transistors were chosen with the minimum channel length of 0.35 $\mu$m except M10 which was chosen 10 $\mu$m.

In this architecture, the auxiliary circuits of both diodes are biased from the output $V_{dc1}$ and driven by the sinusoidal signal at the node $X$ [14]. The pMOS diode is conducting during the positive phase while the nMOS diode is conducting during the negative phase of the input signal. The lowest input voltage $\hat{v}_{ac}$ that can generate a DC-output voltage is determined by the active nMOS diode due to the lower threshold of nMOS transistors: With the input voltage $\hat{v}_{ac} = v_{th,\text{nmos}}$ and the DC-output voltage $V_{dc1} = 0 \, V$, the minimum voltage in node $X$ in the negative phase is $-v_{th,\text{nmos}}$. Provided that the gate of M6 is discharged, the active nMOS diode will start to conduct and raise the DC level at node $X$ by charging $C_{a1}$, so that rectification is activated also in the active pMOS diode.

4.2 Model Verification

The designed voltage multiplier was simulated using Cadence Spectre, with a resonance circuit connected to the multiplier input, so that the required coil voltage for a given output load could be compared to the derived model for DC generation (24). To choose a coil antenna that complies with DC generation using active diodes, the required coil voltage was first compared for different coils as discussed in Section 2.4. In order to plot the required voltage for different coils based on the derived model (24), the term $P_{aux}(V_{dc1})$ was evaluated, as presented in Fig. 10. Based on the result shown in Fig. 11 a coil inductance of 250 $\mu$H was chosen, as the inductance is small enough to allow DC generation with a coil voltage that is comparable to when using ideal diodes.
4. Proposed CMOS Voltage Multiplier

Figure 11: The required coil voltage for multipliers based on FTC and passive diodes, for different values of the coil inductance in the resonance circuit. When increasing the coil inductance, the required coil voltage is increased for FTC diodes while it stays unaffected for passive and ideal diodes as also discussed in Section 2.4. The plots for the passive and ideal diodes are based on (14) with $V_d = 0.7 \, V$ and $V_d = 0 \, V$ respectively. Both the resonance frequency 125 kHz and the Q-factor 50 was the same for all plots.

The maximum number of stages of the multiplier architecture for a supply voltage of 3.5 V was determined by rewriting equation (1) as

Figure 12: Analytical model (24) and Cadence simulation of the required coil voltage $\hat{u}_i$ as a function of N when generating $V_{dc} = 3.5 \, V$ with different load currents of the designed FTC diode based voltage multiplier.
\[
\hat{v}_{ac} = \frac{V_{dc}}{2N} + V_d \approx \frac{V_{dc}}{2N}
\]  

where the FTC scheme has reduced \( V_d \) to nearly zero. For the specified supply voltage, the maximum number of stages was chosen \( N_{\text{max}} = 3 \) so that the input signal \( \hat{v}_{ac} \) exceeds the multiplier threshold voltage \( \hat{v}_{\text{ac th}} \approx 0.5 \) V, to ensure startup. The result of the simulations of the required coil voltage with the chosen coil in Fig. 12 shows that the analytical model is in good agreement with the simulations for multipliers based on active diodes. This confirms that summing the power dissipation of all individual auxiliary components into one term (\( P_{\text{aux}} \)) serves well as a simplification of the model.

4.3 Comparing passive, ITC, and FTC diodes

To compare performance of the designed FTC diode to both passive and ITC diodes, voltage multipliers based on each of the three types of diodes were simulated with a resonance circuit (Fig. 5). The component values of the ITC diodes, shown in Table 2, were chosen based on the design procedure presented in [20], and the multipliers based on passive diodes was simulated using diode connected pMOS transistors with a \( V_{th} \) of typically 0.68 V and a width of 30 \( \mu \)m. DC generation was compared for the multipliers both with and without a current load as shown below, representing both a chip in stand by mode and active mode [2].

Load current \( I_{dc} = 0 \)

The steady-state DC output voltage \( V_{dc} \) was generated at two different coil voltages for up to three cascaded voltage doublers according to Table 3. Included in the table for comparison is the maximum DC output voltage \( V_{dc_{\text{max}}} \). With the Q-factor of 50, the coil

As the output voltages exceed the oxide breakdown voltage 3.5 V of a standard 0.35 \( \mu \)m CMOS process, a HV process is assumed in this example.

<table>
<thead>
<tr>
<th>( N )</th>
<th>( \hat{u}_i )</th>
<th>( V_{dc_{\text{pass}}} )</th>
<th>( V_{dc_{\text{ITC}}} )</th>
<th>( V_{dc_{\text{FTC}}} )</th>
<th>( V_{dc_{\text{max}}} )</th>
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<td>(mV)</td>
<td>(V)</td>
<td>(V)</td>
<td>(V)</td>
<td>(V)</td>
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<td>3.0</td>
</tr>
<tr>
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<td>3.8</td>
<td>4.0</td>
<td>4.9</td>
<td>6.0</td>
</tr>
<tr>
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<td>1.3</td>
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<td>3.7</td>
<td>4.5</td>
</tr>
<tr>
<td>3</td>
<td>30</td>
<td>5.4</td>
<td>5.6</td>
<td>7.0</td>
<td>9.0</td>
</tr>
</tbody>
</table>
5. Measurement Results

The FTC diode based CMOS voltage multiplier was implemented and manufactured in AMS 0.35 μm, 4-metal, 2-poly layer CMOS process. Fig. 14 show a microphotograph...
of the implemented rectifiers including single diode rectifiers and multipliers up to $N = 5$. The chip area of the unit cell marked in the figure is 0.10 mm x 0.17 mm where approximately 50% of the area is occupied by high resistive poly resistors $R_{b1} - R_{b4}$. To reduce area consumption, transistors biased in the subthreshold region can be used as area-efficient high impedance resistors [21].

5.1 Single diode and voltage doubler efficiency

The measurement setup, and the measured power and voltage conversion efficiency of the proposed active diode and the voltage doubler are shown in Fig. 15-17. A significant

![Figure 15: Measurement setup: The chip was mounted on an evaluation board for connection to off chip components $C_{aN}$, $C_{bN}$, an instrumental amplifier and external equipment $V_s$, $I_{dc}$, and OSC.](image)

Figure 14: Micrograph of manufactured chip. Marked on the chip are the unit cell voltage doubler, $N=1$ and a four stage voltage multiplier, $N=4$. 

![Figure 14: Micrograph of manufactured chip. Marked on the chip are the unit cell voltage doubler, $N=1$ and a four stage voltage multiplier, $N=4$.](image)
improvement of the efficiency for rectifiers based on FTC diodes compared to ITC diodes is revealed. For the single FTC diode, an improved PCE compared to the ITC diode is observed with increasing input voltage. This can be explained by the power dissipation due to the DC-bias in $R_b$ that dominates in the ITC diode, but is greatly reduced in the FTC diode where a switched bias is used. The switched bias has a duty cycle of approximately 15%, and the dissipation in $R_b$ depends on the square of the bias current. These factors, in combination, explain the large difference in efficiency that occurs when increasing the input voltage. Interestingly, when comparing the PCE of a single FTC diode with a voltage doubler based on FTC diodes, faster PCE degradation is observed for the doubler despite the use of switched bias. This faster degradation is partly explained by additional power dissipation in $R_{b3}$ and $R_{b4}$ due to the voltage in node $X$ which include a DC component in the doubler architecture [14]. The measured VCEs for the single FTC diode and the FTC based doubler are 89% and 86% respectively, with peak input voltages of $v_{ac} = 0.8$ V and $v_{ac} = 0.5$ V. These values correspond to diode voltages ($V_d$) of 88 mV and 70 mV respectively, which confirm by measurement that full threshold cancellation is achieved in the MOS diodes just above the startup voltage $v_{ac} = v_{th,mos}$ for both rectifiers. Thus, the FTC scheme significantly improves performance where most critical. The corresponding diode voltages ($V_d$) for the ITC based rectifiers are 440 mV and 400 mV, respectively. The larger diode voltage of the ITC diodes also explains the large difference in VCE and PCE at low input voltages for both rectifiers. 

Table 4 provides a comparison of performance of the proposed FTC diode to previously reported active diodes in CMOS. Noticeable is that the proposed FTC diode has a PCE comparable to cited work, but that it achieves this efficiency for a load current that is two orders of magnitude lower than the cited work.

The peak input voltage for the ITC based voltage doubler was $v_{ac} = 0.55$ V.

Figure 16: Measured and simulated PCE and VCE as a function of the peak input voltage of the proposed pMOS active diode. Also shown in the figure, for comparison, is the simulated efficiency of the ITC diode.
5.2 Multiplier DC generation

The performance of the implemented voltage multipliers was verified by generating a DC output voltage of 3.5 V for a range of load currents as shown in Fig. 18. The multipliers were driven by a voltage source with an output resistance of $R_s = 10\, \text{k}\Omega$, based on (13), to mimic the resonance circuit that was used when verifying the analytical model in Fig. 5 and Fig. 12. Given the measured source voltage in Fig. 18, the corresponding coil voltage was calculated based on (12) for $N = 2$ and $I_{dc} = 10\, \mu\text{A}$. A measured source voltage

$$V_s = \frac{V_{out}}{N} \cdot \frac{N^2}{R_s}$$

was used to generate the required source voltage for each load current.
5. Measurement Results

A measurement was performed to test the frequency dependence of an implemented voltage doubler. The measurement showed a 2.6% reduction of $V_{dc}$ at the upper frequency limit of 1 MHz [13], compared to when generating 3.5 V and 10 μA at 125 kHz.

The main contributors to the systematic error in the efficiency measurements (Fig. 16-17) is the accuracy of the instrumental amplifier and the oscilloscope that measure the input current shown in Fig. 19. In comparison, a higher accuracy is expected in the multiplier measurement for $\hat{v}_s$, shown in Fig. 18, as this measurement excludes both of the main sources of error in the measurement setup. The maximal deviations due to systematic error were approximately ±5%, ±1% and ±1% for the measured PCE, VCE and $\hat{v}_s$ respectively.

Table 4: Related work on active diodes in CMOS

<table>
<thead>
<tr>
<th>TCAS II 06 [11]</th>
<th>ISCAS 10 [12]</th>
<th>This work</th>
</tr>
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<tr>
<td>Technology</td>
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<td>0.18μm CMOS</td>
</tr>
<tr>
<td>$\hat{v}_{in}$</td>
<td>1.5V-3.5V</td>
<td>0.7V-1.8V</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>1.2V-3.22V</td>
<td>0.58V-1.68V</td>
</tr>
<tr>
<td>Load</td>
<td>1.8kΩ</td>
<td>500Ω</td>
</tr>
<tr>
<td>PCE</td>
<td>65%-80%</td>
<td>82%-87%</td>
</tr>
<tr>
<td>Frequency</td>
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<td>10kHz-1.5MHz</td>
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</table>
6 Conclusion

A DC generation model for inductive RFID tags has been presented. The analytical model was derived for a voltage multiplier driven by a resonance circuit while meeting requirements for supply voltage and current. Comparisons of the model to simulations in Cadence Spectre show good agreement with the model for multipliers based on both passive and active diodes in CMOS. Several design examples for maximized DC generation were presented based on the model. Also presented were the design and implementation of a voltage multiplier in CMOS based on active diodes. Measured performance of the manufactured CMOS multiplier shows good agreement with both the simulations and the derived model.

References


A CMOS Front-end for RFID Transponders Using Multiple Coil Antennas

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A CMOS Front-end for RFID Transponders Using Multiple Coil Antennas

Hans Rabén, Johan Borg and Jonny Johansson

Abstract

A front-end architecture for inductive RFID transponders using multiple coil antennas for reduced orientation sensitivity is presented. The front-end uses multiple antennas for reception and one antenna for transmission. A select function identifies the antenna that is most favorably oriented toward the reader for transmission by comparing the DC charge-up phases of multiple DC generation blocks during power-up of the transponder. Design, simulations and measurement results of a front-end manufactured in 0.35 μm CMOS for 125 kHz FSK modulation are presented for a pulsed RFID system as well as an architecture for cascaded DC generation. This paper also includes an example of a coil antenna for spherical transponders using three independent orthogonal windings.

1 Introduction

RFID technology is used in many applications for tracking and tracing in the supply chain as well as in the process industry [1–3]. One factor that limits readability when tracing moving objects that are arbitrarily oriented toward a reader antenna is the orientation sensitivity of the transponders [4–6]. It is possible to reduce the orientation sensitivity in an inductive RFID system using transponders with multiple coil antennas so that simultaneous reception in multiple directions is enabled. In addition to orientation sensitivity, the readability is also affected by the communication technique used between the reader and the transponder. To improve the readability of inductive transponders, a pulsed RF signal is commonly used for communication. In the pulsed system, also known as the sequential system, an RF burst is sent from the reader to power-up the transponder. When the burst ends, the transponder uses a local oscillator to send an FSK modulated message back to the reader. The main advantage compared to when using a continuous RF signal in combination with conventional load modulation is that the RF signal in the reader coil is turned off before receiving the telegram from the transponder. This typically improves the signal-to-interference ratio by 20 dB, which has a positive effect on the system reading range [7]. Thus, a transponder using multiple coil antennas and a pulsed communication technique is a promising candidate for improving readability when tracing moving objects. However, in contrast to radiative RFID, which allows for simultaneous transmission from multiple antennas [8], one of the coil antennas needs to be selected for transmission in an arbitrarily oriented transponder. This is to avoid negative interference between the transmitted magnetic fields, which may result in magnetic field...
cancellation at the location of the reader antenna. In addition to reduced orientation sensitivity, using multiple antennas offers the possibility to power the transponder with multiple RF-to-DC conversion blocks connected in cascade [9].

Fig. 1 shows an 11 mm antenna for 125 kHz RFID transponders with three independent coils. This antenna uses 220 turns of 100 μm wire to realize an inductance of approximately 700 μH, and the antenna exhibits a coupling (k) between the coils of less than 0.004. Winding the coils on a hollow polymer support allows an integrated circuit to be placed within the coil before the coil is filled and encased by a suitable polymer. Filling this polymer with a suitable high-density material (e.g., tungsten powder or lead oxide) allows the density of the transponder to be adjusted to avoid segregation between transponders and the product [10].

In this paper, front-end design in 0.35 μm CMOS for inductive transponders using multiple antennas for reception and a single antenna for transmission are presented. A select block is designed to select the antenna that is most favorably oriented toward the reader for transmission. The select block is used in the design of a front-end in 0.35 μm CMOS for FSK modulation as well as an architecture for cascaded DC generation.

In Section 2 of this paper, the design of the select block is presented. Sections 3-4 present the design and simulation results for FSK modulation as well as for the cascaded DC generation. In Section 5 measurements on the select block, FSK front-end and the architecture for cascaded DC generation are presented before the paper is concluded in Section 6.
2. **Select**

To take advantage of multiple coil antennas, a function block that selects one antenna for transmission was designed. The select block shown in Fig. 2 compares the DC charge-up phases of the three rectifier blocks during power-up of the transponder to identify the antenna with the strongest incoming signal. Three level detectors are driven from the outputs of the rectifier blocks and generate a step output voltage as the input voltage reaches the detection level. A 3-way mutex is used to determine which of the three detector signals arrives first so that a high-output signal is generated only for the antenna receiving the strongest signal from the reader.

2.1 **Level detector**

The level detector includes a current mirror and a pMOS common source stage, as shown in Fig. 3 a). As the input voltage $V_{dc}$ increases, the diodes $P1$, $P2$ and $N1$ in the current mirror start to conduct. The resulting voltage drop on the MOS resistor $P3$ activates the pMOS stage $P4$, which uses an active load $N3$ to maximize the gain and improve the step characteristics of the detector output voltage. The buffer stage in Fig. 3 b) includes an nMOS common source stage $N5$ with an active load $P6$ and a CMOS inverter $P7$, $N6$. The purpose of the buffer stage is both to further improve the step characteristics and to ensure that the three inputs of the mutex are always driven with $V_{dd}$ as the active high level. Included, but not shown in the figure, are two nMOS current sources parallel to $N4$ biased from $vb1$ of the second and third detector so that the pMOS loads in all buffers can be biased from $vb2$. This arrangement avoids output distortion from a buffer when it is powered-up without an input signal.
2.2 3-way mutex

A multi-way mutex is commonly used in digital systems where there is a need for arbitration between competing asynchronous input signals. For this application, a 3-way mutex based on cross-connected latches is chosen because it is recommended for low-latency operation [11]. The latches are based on three-input NAND gates and on output inverters, as shown in Fig. 4. The operation of the mutex, also called the arbiter, is further described in [12] [13].

3 FSK modulation front-end

This section presents the design and simulation results of an FSK modulation front-end for transponders using multiple antennas in a pulsed RFID system, as shown in Fig. 8.

3.1 End-of-burst detector

In a pulsed RFID system, the end-of-burst detector is used to detect when the signal sent from the reader to power the transponder is turned off. The end-of-burst detector shown in Fig. 5 is based on [14,15] and is here modified to be used with a balanced rectifier. The detector includes a capacitive output stage as an alternative to the proposed hysteresis function. During the RF burst, the current source $P2$ charges capacitor $C1$ at the same time as the RF peak voltage periodically turns on transistor $P3$ so that $C1$ is discharged and so that $P4$ is prevented from turning off. At the end of the burst, the RF peak is reduced, which allows the capacitor $C1$ to be charged, $P4$ to turn off and the output stage $P5$ to turn on so that the capacitor $C2$ is charged. A buffer stage $N4, N5, P6$ and $P7$ is included to improve the step characteristics of the EOB signal. Transistor $N3$ is driven by a reset signal $R$ that discharges $C2$ at the end of the transmission phase of the transponder.

![Figure 3: a) The level detector, including b) an output buffer supplied by $V_{dd}$. A step voltage $V_{out}$ is generated during DC charge-up at the detection level $V_{det} = V_{dc} \approx V_{thP1} + V_{thP2} + V_{thN1}$ with a typical rail-to-rail rise time of 1 μs, which ensures power-efficient operation in the digital mutex.](image-url)
3. Modulation and rectification

At the end of the burst, the transponder uses a local oscillator to send an FSK modulated signal back to the reader. In this design, as shown in Fig. 6, a differential cross-coupled oscillator topology is chosen using one pMOS pair $P_1$, $P_2$ and one nMOS pair $N_5$, $N_6$ to drive the resonance circuit $L$, $C_R$ [16]. The switches $N_1$, $N_2$ are driven by the data signal and are used to achieve frequency shift keying by switching the capacitors $C_1$, $C_2$ in parallel with the resonance circuit. Because the chosen oscillator topology is related to the topology of the balanced bridge rectifier, here the oscillator and the rectifier blocks are combined into one common block with two modes of operation. The rectifier block uses the pMOS pair $P_1$, $P_2$ together with an additional pair of nMOS diodes $N_3$, $N_4$ [17].

During power-up of the transponder when a select signal is generated, the Data and EOB signals are low so that the biasing and the frequency shift keying of the oscillator are disabled. In this mode, rectification of the incoming signal from the resonance circuit is achieved. At the end of the burst when the incoming power signal from the reader is turned off, the mode of operation is changed from rectification into oscillation as the EOB and Data signals are activated. One advantage of combining the two circuits is that the need to switch the resonance circuit between the two blocks is avoided.
To achieve multi-stage DC generation, the rectifier block presented in Fig. 7 may be
3. FSK modulation front-end

Figure 8: FSK modulation front-end, including the antenna select function for transmission as well as FSK modulators and end-of-burst detectors (the combined FSK modulator and rectifier are shown as separate blocks).

added to the combined block. By connecting the output $v_{ob}$ between $N_y$ and $N_z$ instead of to the ground as reference, as well as connecting the AC coupling capacitors to $V_+$ and $V_-$, the added rectifier will serve as the input stage in a two-stage rectifier topology, as further described in [18]. It is worth noting that during the oscillation mode, the input stage will generate DC, which, at the same time, is consumed by the oscillator. However, this may cause extra loading of the resonance circuit for larger N-stage topologies due to additional power dissipation in the diodes $N_1-N_4$. 
Figure 9: A pMOS full threshold cancellation diode (FTC) presented in [19]. The diode voltage $V_d$ is approximately 50 mV for the output current $I_{dc} = 10 \mu A$.

3.3 Front-end design

The FSK modulation front-end shown in Fig. 8 includes three DC generation blocks driven by the coil antennas $L_x$, $L_y$ and $L_z$. By using three diodes, the outputs of the DC generation blocks are combined into one common output voltage $V_{dd}$ that supplies the circuits on the transponder chip as well as the select block in the front-end. This allows all circuits to be supplied by the largest of the three generated DC voltages, here called single antenna DC generation. To minimize the additional voltage drop after the AC-to-DC conversion, active FTC diodes are used here [19]. The FTC diode shown in Fig. 9 is optimized to enable a low current consumption so that loading effects on the resonance circuits are minimized. The inputs of the select block are connected to the storage capacitors $C_s$ of the rectifier blocks for level detection of the DC charge-up phases during power-up of the transponder, as described in Section 2. When the front-end receives a power burst from the reader, a select signal is generated during the DC charge-up phase. As the reader is turned off, an EOB signal (or several) is generated so that both the or-switch and the selected FSK modulator are activated. This allows the

Figure 10: Or-switch including a pass-transistor P1, active load P2 and nMOS switches N1-N3.
chip to power-up for data generation in the digital back-end of the transponder chip at the same time as an FSK modulator is biased. The or-switch is shown in Fig. 10.

Figure 11: Simulation results of the FSK modulation front-end driven by three antenna signals with different amplitudes.
Table 1: Component values

<table>
<thead>
<tr>
<th>Component</th>
<th>N1 (µm)</th>
<th>N2 (µm)</th>
<th>N3 (µm)</th>
<th>N4 – N6, P4 – P6 (µm)</th>
<th>P1, P2, P7 (µm)</th>
<th>P3 (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level Detector</td>
<td>5</td>
<td>2</td>
<td>50</td>
<td>2</td>
<td>5</td>
<td>W=1, L=300</td>
</tr>
<tr>
<td>FTC Diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P1, P3, P5, P2, P4, N1, N2, N3</td>
<td>1</td>
<td>100</td>
<td>1</td>
<td>5</td>
<td>2</td>
<td>15</td>
</tr>
<tr>
<td>EOB Detector</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P1, P2, P5, N2, N3 – N5, P3, P4, C1, C2, N1 (µm)</td>
<td>50</td>
<td>2</td>
<td>50</td>
<td>5</td>
<td>1.5</td>
<td>W=1, L=300</td>
</tr>
<tr>
<td>FSK Modulator</td>
<td>L (mH)</td>
<td>C_R (pF)</td>
<td>R1 (kΩ)</td>
<td>P1, P2, N1, N2, N3 – N7, C1, C2 (µm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5</td>
<td>648</td>
<td>5</td>
<td>50</td>
<td>50</td>
<td>20</td>
</tr>
<tr>
<td>Single to Cascade</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N1 (µm)</td>
<td>N2 (µm)</td>
<td>N3 (µm)</td>
<td>P1 – P3 (µm)</td>
<td>P4 – P6 (µm)</td>
<td>P6 – P9 (µm)</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>100</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

Transistor sizes are for the width W. All transistors, except where stated, have the minimum channel length (0.35 µm).

3.4 RF limiter

The front-end uses RF limiters connected in parallel with each resonance circuit for voltage clamping when the incoming electromagnetic field is too strong. Here, the limiter presented in [20] is designed so that RF limitation starts at approximately 2.5 V. This prevents the RF peak input voltage from exceeding the 3.6 V breakdown voltage of the CMOS process and starts limiting the rectifier output voltage above the detection level $V_{det}$. This gives an unregulated supply voltage $V_{dd}$ of approximately 1.8 - 3 V. Additional $V_{dd}$ limitation may be achieved by adding a large nMOS transistor biased from $v_b$ and connected in parallel with $P1$, $P2$ and $N1$ of the level detector.

3.5 Front-end Simulation

The function of the designed FSK modulation front-end was verified for a pulsed low-frequency (LF) RFID system. The included circuit blocks were implemented in 0.35 µm.
CMOS, and resonance circuits at 125 kHz with an unloaded Q-factor of 50 were designed, with component values as shown in Table 1. The capacitors $C_1$ and $C_2$ in the combined FSK modulator and rectifier block were chosen to generate 10% frequency shift keying of the carrier signal during the transmission from the transponder at a chosen data rate of 4 kb/s. The resonance circuits were driven with continuous RF signals with different amplitudes to verify that the select function allows power-up as well as modulation using the antenna receiving the strongest signal. The induced RF signals in the coil antennas were simulated using an ideal voltage source connected in series to each coil. Here, an incoming RF burst of 10 ms with the induced peak voltages $\hat{u}_x = 80 \, \text{mV}$, $\hat{u}_y = 70 \, \text{mV}$ and $\hat{u}_z = 60 \, \text{mV}$ was used to power-up the transponder. The simulation results in Fig. 11 show that a select signal $x$ is generated for $V_{dcx}$ during the DC charge-up phase of the transponder. When the antenna signal is turned off at 10 ms, an FSK modulated message is sent by the selected antenna after the EOB signal is generated. A fast decay of the amplitude of the modulated signal can be seen due to the relatively small storage capacitor used here to supply the power-hungry oscillator: A voltage drop of approximately 1 V during a transmission phase of 3.1 ms and a storage capacitor of 50 nF yields an average current of 17 $\mu$A in the FSK modulator. It can be observed in the figure that the peak amplitude of the oscillation is approximately equal to $V_{dcx}$ during the transmission and that the difference between the peak voltage of the RF burst and $V_{dcx}$ is approximately 0.5 V due to the voltage drop of the nMOS diode in the bridge rectifier.

4 Cascaded DC generation

The concept of cascaded DC generation is shown in Fig. 12, where the DC generation blocks are connected in series with a common storage capacitor that is charged from the outputs of each rectifier block [9]. In contrast to the single antenna DC generation presented above, where two out of the three DC generation blocks are unused, the cascade allows the generated DC from all blocks to be summed on a common load.

4.1 Cascaded DC generation architecture

The architecture for cascaded DC generation is shown in Fig. 13, where a circuit block for conversion from single antenna to cascaded DC generation is combined with the select function. The purpose of this architecture is both to identify one antenna for transmission and to supply the transponder chip with the summed voltage from three DC generation blocks. For example, this enables the possibility to use cascaded DC generation in the front-end presented above. The conversion block is activated after a select signal has been generated during DC charge-up of the transponder and connects the capacitors in series to the storage capacitor $C_s$ via the or-switch. The conversion is performed after the select function because the select function requires the DC charge-up phases to be compared during single antenna DC generation because the charge-up in each stage will be biased by each other when connected in cascade. The capacitors $C_x$, $C_y$ and $C_z$ are
Figure 12: Cascaded DC generation topology using three antennas.

chosen to be small compared to $C_s$ so that the charge-up time for the select signal has a negligible impact on the total charge-up time.

**Single-to-cascade conversion**

The single-to-cascade conversion block is shown in Fig. 14. The block is activated by a select signal and connects the capacitors in series, where the initially selected capacitor remains connected to ground. This simplifies the cascading of the capacitors if one or two out of the three capacitors are uncharged because the pMOS switches require a positive potential on the source to conduct. The function of the different components in the block are briefly described for capacitor $C_x$ as follows: Switch $N1$ is used to disconnect $C_x$ from ground, while the switches $P2$ and $P3$ connect $C_x$ to the capacitor $C_y$ or $C_z$, and switch $P1$ disconnects $C_x$ from the input of the select block. The NOR gate $I3$ controls switches $N1$ and $P1$, and the buffer stage $I1$ (Fig. 3 b) is used to prevent switch $P3$ or $P5$ from closing before the ground switch $N1$ is opened.

The function of the block is further explained below by describing the single-to-cascade conversion for the case when select $x$ is generated: During DC charge-up when a select signal is generated for $x$, the output state of the NOR gates $I6$ and $I9$ changes from high to low so that the two ground switches $N2$ and $N3$ open and disconnect capacitors $C_y$ and $C_z$ from ground. At the same time, the output state of the buffer $I4$ changes from high to low so that switches $P6$ and $P8$ close and connect node $V_{dc|x}$ to $C_y$ as well as node $V_{dc|x}$ to $C_z$ so that the two capacitors are connected in series with $C_x$. To avoid loading of the cascade, switches $P4$ and $P7$ are closed so that $C_y$ and $C_z$ are disconnected from the input to the select block. To allow the detectors to be disconnected, two additional current sources were connected in parallel to both $N1$ and $N3$ so that all FTC diodes
are biased from $v_{b_1}$ in each level detector.

4.2 Simulation of Cascaded DC generation

Cascaded DC generation was simulated using the same LF resonance circuits as discussed in Section 3.5 together with single-diode rectifiers with output capacitors of 250 pF and with a storage capacitor $C_s = 2.5$ nF. Three different simulations were performed, as described below.

1) Three antennas with different voltage levels chosen as $\hat{u}_{i_x} = 20$ mV, $\hat{u}_{i_y} = 30$ mV and $\hat{u}_{i_z} = 40$ mV were used to generate a theoretical summed voltage of 3 V, given a Q-factor of 50 and a total diode voltage drop of approximately 1.5 V. See Fig. 15 (top).

2) Three antennas with equal voltage levels chosen as $u_{i_x} = u_{i_y} = u_{i_z} = 40$ mV were used to generate a theoretical summed voltage of 4.5 V. See Fig. 15 (middle).

3) One antenna with the voltage level chosen as $u_{i_x} = 40$ mV while $u_{i_y} = u_{i_y} = 0$ mV was used to generate a theoretical summed voltage of 1.5 V. See Fig. 15 (bottom).

![Figure 13: Cascaded DC generation architecture, including the antenna select function. The total current consumption of the architecture is less than 0.2 μA at a generated supply voltage of $V_{dd} = 2.5$ V](image-url)
The simulation result in Fig. 15 shows that after a short charge-up phase that generates the select signal, a voltage drop occurs as the capacitors $C_x$, $C_y$, and $C_z$ are connected in series and in parallel with a 10-times-larger load capacitor. At the end of the charge-up phase, a difference of approximately 0.5 V is found between the cascaded output voltage and that in the ideal case, despite a total voltage drop on the switches and the FTC diodes of less than 100 mV. Additional simulations showed that this difference is caused by a reduced Q-factor in the resonance circuits due to the total current consumption of the front-end, which creates three times as much power dissipation in the rectifier blocks as the same load current does in one rectifier.

5 Measurement results

The circuit architectures presented above were implemented and manufactured in a 0.35 μm 4-metal, 2-poly layer CMOS process. In Fig. 16, a micrograph of the manufactured chip is shown, with the implemented FSK front-end. The areas of the FSK front-end, the select block and the block for cascaded DC generation are approximately 490x230 μm, 240x210 μm and 330x220 μm, respectively. All of the components of respective block, except for the storage capacitors and the input resonance circuits, were implemented on
Figure 15: Simulations of the designed architecture for cascaded DC generation for three cases, with the coil voltages chosen as described in Section 4.2.

5.1 Select block measurement

The function of the select block shown in Fig. 2 was verified as follows. To generate DC charge-up phases on the storage capacitors, each rectifier input was driven by a generator with a sinusoidal signal at 125 kHz and a source resistance of 10 kΩ. On-chip single pMOS diode rectifiers were used with storage capacitors of 47 nF. The generators were synchronised to start simultaneously. The measurement result shown in Fig. 17 indicates that a select signal $z$ is generated for the signal generator with the largest amplitude, $V_z = 3.0$ V. A corresponding simulation showed good agreement with the characteristics of the measured signals $x$, $y$, $z$ and $Vdd$, as presented in Fig. 17.
5.2 FSK front-end measurement

The measurement of the FSK front-end was set up to mimic the simulation performed in Section 3.5, where RF bursts were induced in the input resonance circuits. To mimic the resonance circuits in Fig. 8, one signal generator for each rectifier input was used. Each signal generator was transformer-coupled to the rectifier input. A capacitor $C_R$ of 740 pF was connected on the secondary side to resonate at 125 kHz with an inductance $L$ of...
2.2 mH of the secondary winding. The source resistance of the signal generator was chosen to achieve an unloaded Q-factor of 50 of the resonance circuits. After synchronising the generators to start simultaneously and setting the signal amplitudes, RF bursts were induced in each resonance circuit. The measured results in Fig. 18 show the differential voltage \( V_x \) of coil \( L_x \) for two different amplitude settings: In the upper figure, the signal amplitudes were set to generate a measured RF burst with a maximum peak voltage of approximately 1.8 V, 1.5 V and 1.5 V for coils \( L_x, L_y \) and \( L_z \) respectively. In the lower figure, the corresponding peak voltages were 1.5 V, 1.8 V and 1.5 V, respectively. The results show that after the RF burst, during the transmission phase of the transponder, a short oscillation is generated in coil \( L_x \) when it receives the strongest signal. In contrast, when coil \( L_y \) receives the strongest signal, no oscillation occurs in coil \( L_x \). While the measurement verifies the select function of the front-end, a simulation showed that the duration of the measured oscillation is approximately 30 % shorter than expected. This difference may be attributed to increased bias current in the oscillator: The bias resistor \( R_1 \) was implemented as a high-resistive poly resistor with a size below the recommended minimum size, which may have resulted in a lower value and a faster discharge of the
Figure 19: Measurement result of the cascaded DC generation block for the three cases presented in Section 4.2. The individual voltages $V_{dcx}$, $V_{dcy}$ and $V_{dcz}$ and the summed output voltage $VDD$ are shown in the figure.

5.3 Cascaded DC block measurement

The measurement of the architecture for cascaded DC generation was performed in the same manner as described for the FSK front-end, where transformer-coupled signal generators were used to mimic the simulation of induced signals in the resonance circuits. Rectification was achieved using on-chip single pMOS diode rectifiers with output capacitors of 330 pF and with a storage capacitor of 3.3 nF. For comparison with the simulation results presented in Fig. 15, three measurements were performed; the signal levels of the generators were chosen so that the induced coil voltage corresponded to the three cases.
presented in Section 4.2. The measurement results presented in Fig. 19 show that cascading of the output voltages $V_{dcx}$, $V_{dcy}$, and $V_{dcy}$ is achieved after a short charge-up phase, in agreement with the simulations. However, the results also show that the value of the summed output voltage in the steady-state is lower in the measurement. A comparison with simulation indicates that this deviation can be attributed to the additional loads of the probes used in the measurement, which reduce the loaded Q-factor of the resonance circuits, as discussed in Section 4.2.

6 Conclusion

A front-end for an inductive RFID transponder using multiple coil antennas was presented. Circuit solutions in CMOS for achieving multiple antenna reception and single antenna transmission were designed. Simulation results were presented, in which 125 kHz FSK modulation for a pulsed RFID system as well as cascaded DC generation was achieved with the designed front-end. The circuit performance was verified by measurements on manufactured circuits. An example of a multiple coil antenna for spherical RFID transponders was also presented in this paper. The presented circuit solutions are, to the best of our knowledge, the first for inductive RFID transponders using multiple coil antennas. The results demonstrate potential for facilitating the use of RFID in harsh environments.

7 Acknowledgements

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References


