Design of a Coprocessor Board for an On Board Computer

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Abstract

The goal of this thesis is to design a coprocessor expansion board for an On Board Computer (OBC) using Commercial Off The Shelf (COTS) components. This is done in order to meet the increasing demand of more processing power as spacecrafts become more autonomous. After evaluating a number of different options, the LS1046A from ARM was chosen as the processing unit. This would increase the processing power from the current 110 Dhrystone Million Instructions Per Second (DMIPS) to a theoretical 22 560 DMIPS. The schematic was designed in DxDesigner, and after the layout was completed signal integrity simulations were performed in HyperLynx. After modifications to termination resistances, the simulations showed good signal integrity confirming proper routing of the signals. After receiving the manufactured Printed Circuit Board (PCB) with all components mounted, some tests could be performed confirming that the power distribution and the system clock was functioning properly.
Acknowledgements

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Thank you to our supervisor Jonas Mörfeldt for all the help and guidance during this thesis. Also thanks to all of the people at RUAG who have had the patience to help and to answer all of our questions.

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Abbreviations

AMD Advanced Micro Devices
ASIC Application Specific Integrated Circuit
COTS Commercial Off The Shelf
CPU Central Processing Unit
DDR Double Data Rate
DIMM Dual In-line Memory Module
DMIPS Dhrystone Million Instructions Per Second
FPGA Field-Programmable Gate Array
GPU Graphics Processing Unit
I2C Inter-Integrated Circuit
IC Integrated Circuit
JTAG Joint Test Action Group
MCM Multi-Chip Module
MCU Micro Controller Unit
OBC On Board Computer
OBC NG Next Generation On Board Computer
ODT On-Die Termination
PCB Printed Circuit Board
PCIe Peripheral Component Interconnect Express
POR Power on Reset
QSPI Quad Serial Peripheral Interface
RAM Random Access Memory
RCW Reset Configuration Word
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
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<tr>
<td>SBC</td>
<td>Single Board Computer</td>
</tr>
<tr>
<td>SerDes</td>
<td>Serializer/Deserializer</td>
</tr>
<tr>
<td>SF2</td>
<td>SmartFusion2</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon On Insulator</td>
</tr>
<tr>
<td>SPD</td>
<td>Serial Presence Detect</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SpW</td>
<td>SpaceWire</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random Access Memory</td>
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<tr>
<td>TDP</td>
<td>Thermal Design Power</td>
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Chapter 1

Introduction

Processors, and other electronics, used in space applications need to be able to withstand the harsh environment in which they will operate. That is why mostly well tested radiation hardened components, that have been proven to be able to survive, are used. This has the implication, however, that these components are relatively old and outdated.

Now there is an ever increasing demand for more processing power as satellites, probes and rovers are required to perform more and more complicated tasks (e.g. autonomous manoeuvres like docking, landing and navigating on planets and moons). Because of this, many companies in the space industry have now started to look at so called Commercial Off The Shelf (COTS) products for use in space applications in order to meet this growing demand. The downside of using COTS products, however, is that they lack the heritage and the extensive radiation tests of standard space qualified components.

1.1 The On Board Computer

The Next Generation On Board Computer (OBC NG), Fig. 1.1, is developed by RUAG Space and uses a radiation hardened Application Specific Integrated Circuit (ASIC), named CREOLE, as its main processor [1]. The processor is operating at a frequency of 87.5 MHz, producing 110 Dhrystone Million Instructions Per Second (DMIPS).
The OBC NG is a fully redundant system that can be scaled to different configurations using expansion slots, Fig. 1.2. These can be used to add functionalities like a Global Navigation Satellite System (GNSS) receiver and additional mass memory (MM). One of these slots are used for the board housing the CREOLE (called the CM card), on to which a mezzanine board with a coprocessor can be mounted. This coprocessor will be able to communicate with the CREOLE using SpaceWire (SpW) or Serial Peripheral Interface (SPI).

Figure 1.1: The OBC NG module with two expansion slots [1].

![OBC NG module with two expansion slots]

Figure 1.2: Block diagram of the OBC NG with two expansion slots [1].
The OBC NG will be referred to simply as "On Board Computer" (OBC) for the remainder of this report.

1.2 Objectives & Goals

The goal of the thesis is to design a coprocessor expansion card for the OBC, to provide an option to significantly increase its processing power.

The objectives of the thesis are:

- Choosing a suitable processor and memory to be used.
- Designing the printed circuit board.
- Testing and evaluating it on the on board computer.
Chapter 2

Components

This thesis only aims to create a prototype version of the coprocessor board and evaluate it, however, if this project is to be expanded upon, and an actual flight model is to be developed based on this thesis, the space viability of the components used needs to be taken into account. Listed below are a few guidelines used to aid in the selection of suitable components.

- The processing power should ideally be no lower than 5000 DMIPS.
- The components should be cheaper than radiation hardened alternatives currently in use.
- Low power consumption.
- Has any radiation testing been done, or has it been used previously in space environments.

2.1 CREOLE and Coprocessor Communication

As the CREOLE in the OBC only supports SpW and SPI, the simplest solution for the communication would be to use a coprocessor that supports one, or both, of these communication protocols. Of these two protocols, SpW is the preferred option due to its larger bandwidth. When it comes to modern COTS-processors, which do not usually support SpW, the SPI interface does not support a high enough bandwidth in order to utilize the full potential of these processors in this application. However, RUAG have, for previous projects, developed a solution for converting a Peripheral Component Interconnect Express (PCIe) signal to SpW using a Field-Programmable Gate Array (FPGA). This solution could be utilised in this project as well, allowing the use of PCIe as a communication protocol.
2.2 Selecting Processing Unit

The selection process involved looking at a large number of alternatives for the processing unit and narrowing down the list by evaluating different criteria until an optimal candidate had been found. These criteria involved, for instance: Processing power, cost, radiation tolerance, interfaces for communicating with the OBC and power consumption. Processing units with processing speeds several orders of magnitude above what is currently in use in the OBC are readily available on the market, and so the decision was made to primarily evaluate processing units with some sort of radiation tolerance or previous heritage in space missions.

2.2.1 Graphics Processing Unit

The idea of using a Graphics Processing Unit (GPU) as the processing unit was considered because it would most likely reach a processing power well above the minimum requirement for this application. However, due to the apparent lack of space qualified GPUs available on the market as well as a lack of heritage for GPUs in space applications, the idea was quickly dismissed.

2.2.2 Microcontroller

Micro Controller Units (MCUs) provide some advantages for an application such as this. For instance, Random Access Memory (RAM) is integrated in the unit. This tends to save both time and money for the developer, who no longer needs to acquire and integrate a separate RAM module. MCUs also tend to be a cheaper option compared to a processor and external RAM. MCUs come with a notable disadvantage though, mainly in the lack of processing power. A small number of space graded MCUs using Static Random Access Memory (SRAM) were evaluated and the result can be seen in Tab 2.1.

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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ATmegaS64M1</td>
<td>8</td>
<td>8.88</td>
<td>4KB SRAM</td>
<td>SPI</td>
<td>[2]</td>
</tr>
<tr>
<td>Vorago VA10820</td>
<td>63.5</td>
<td>0.203</td>
<td>32KB SRAM</td>
<td>SPI</td>
<td>[3, 4]</td>
</tr>
<tr>
<td>SAM V71</td>
<td>600</td>
<td>1.7</td>
<td>384KB SRAM</td>
<td>SPI</td>
<td>[5]</td>
</tr>
</tbody>
</table>

The max power is estimated based on the maximum voltage allowed and the maximum current load in the worst case scenario for each MCU. Even though SpW or PCIe are preferable when communicating with the CREOLE, SPI is also an option. As the goal of this project is to significantly improve the processing power of the CREOLE (110
DMIPS), and the most promising candidate only provides a slight increase in processing power (600 DMIPS), neither of these components are a realistic choice, and were thus disregarded.

2.2.3 Processor

For many space applications, using a processor with external RAM, usually Double Data Rate (DDR) memories, is a common solution, and thus there exist a large pool of relevant devices to choose from. As stated earlier, because the processing power of COTS-processors are usually well above the target processing power of this application, the choice was made to primarily focus on processors which had been tested for some kind of radiation or qualified for space applications in some way.

A company called Teledyne-e2v provides upscreening and radiation tests for COTS-processors, and RUAG has a history of cooperating with them in the past. Teledyne-e2v offers different series of processors, and a variety of processors ranging from slow with low power consumption to faster and more power hungry were selected as potential candidates. A small selection of processors from Intel and Advanced Micro Devices (AMD) have also been considered as there has been radiation tests performed on some of their processors [6].

The idea of using radiation-hardened (rad-hard) processors were also investigated, especially some newer ones who might reach the target performance, although rad-hard components might be to costly for this application.

A total of 17 processors were found as potential candidates. These are presented fully in Appendix A and as a short list containing the most relevant information in Tab. 2.2.
### Table 2.2: Processors evaluated

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</tr>
</thead>
<tbody>
<tr>
<td><strong>Teledyne e2v</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Arm LS1088A</td>
<td>29440</td>
<td>9.6</td>
<td>PCIe</td>
<td>DDR4</td>
<td>[7, 8]</td>
</tr>
<tr>
<td>Arm LS1046A</td>
<td>33840</td>
<td>20.5</td>
<td>PCIe</td>
<td>DDR4</td>
<td>[9, 10]</td>
</tr>
<tr>
<td>PowerPC T2080</td>
<td>43200</td>
<td>24.8</td>
<td>PCIe</td>
<td>DDR3/3L</td>
<td>[11, 12]</td>
</tr>
<tr>
<td>PowerPC PC8572E</td>
<td>6897</td>
<td>25.9</td>
<td>PCIe</td>
<td>DDR2/3</td>
<td>[13]</td>
</tr>
<tr>
<td>PowerPC PC7448</td>
<td>3000</td>
<td>12</td>
<td>Not integrated</td>
<td>DDR2/3</td>
<td>[14]</td>
</tr>
<tr>
<td>PowerPC P1013</td>
<td>2880</td>
<td>4.75</td>
<td>PCIe</td>
<td>DDR2/3</td>
<td>[15]</td>
</tr>
<tr>
<td>PowerPC P2020</td>
<td>6118</td>
<td>7.2</td>
<td>PCIe</td>
<td>DDR2/3</td>
<td>[16]</td>
</tr>
<tr>
<td>PowerPC PC8548E</td>
<td>3065</td>
<td>12.8</td>
<td>PCIe</td>
<td>DDR/2</td>
<td>[17]</td>
</tr>
<tr>
<td>PowerPC P4040</td>
<td>13800</td>
<td>27.6</td>
<td>PCIe</td>
<td>DDR2/3</td>
<td>[18]</td>
</tr>
<tr>
<td>PowerPC P1011</td>
<td>1840</td>
<td>2.65</td>
<td>PCIe</td>
<td>DDR2/3</td>
<td>[19]</td>
</tr>
<tr>
<td>PowerPC P1020</td>
<td>3680</td>
<td>3.08</td>
<td>PCIe</td>
<td>DDR2/3</td>
<td>[20]</td>
</tr>
<tr>
<td><strong>Rad Hard</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GR740</td>
<td>1840</td>
<td>1.8</td>
<td>SpW</td>
<td>PC100</td>
<td>[21, 22]</td>
</tr>
<tr>
<td>PowerPC RAD5545</td>
<td>5600</td>
<td>17.7</td>
<td>SpW</td>
<td>DDR2/3</td>
<td>[23]</td>
</tr>
<tr>
<td><strong>Other</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Arm LS2044A</td>
<td>37600</td>
<td>25.8</td>
<td>PCIe</td>
<td>DDR4</td>
<td>[9, 24]</td>
</tr>
<tr>
<td>Intel Core i3-5005U</td>
<td>-</td>
<td>15</td>
<td>PCIe</td>
<td>DDR3L</td>
<td>[25]</td>
</tr>
<tr>
<td>Intel Pentium III</td>
<td>1595</td>
<td>29</td>
<td>N/A</td>
<td>-</td>
<td>[26, 27]</td>
</tr>
<tr>
<td>AMD A4-3300</td>
<td>-</td>
<td>65</td>
<td>PCIe</td>
<td>DDR3</td>
<td>[28]</td>
</tr>
</tbody>
</table>

The maximum power in the table above is the Thermal Design Power (TDP) when run at the highest temperature allowed specified by each device’s allowed temperature range. The DMIPS values are rough estimates, based on either existing data or estimated based on data found for devices with a similar architecture. For devices where the processing power was given in DMIPS/MHz, the total estimated processing power was calculated by multiplying that number with the frequency of the processor and the number of cores.

For both LS1046A and LS2044A the DMIPS in Tab. 2.2 were calculated using values found on Wikipedia, as those were the only values of DMIPS found for these processors. Although Wikipedia might not be the most reliable source of information, these values can still give an estimate to the processing power for the two processors.

Another value that can be used to compare the processing power of different processors is their CoreMarks. The LS1046A has a CoreMark value of around 45000 [29], which can be compared to the GR740 which has a CoreMark Value of around 2100 [30]. This CoreMark comparison shows that the DMIPS values used for the LS1046A and the LS2044A (which uses the same core) in the table above should be accurate enough to

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be able to be used in the selection process of the processors.

### 2.2.4 Narrowing Down the Selection

The processors manufactured by Intel and AMD appear to be poor choices for this application, as information regarding these products is hard to come by. Additionally, the Intel-processors are old enough to be discontinued by their manufacturer [31]. This makes the Intel processors far from ideal for this application and can thus be disregarded, especially Intel Pentium III since it does not possess the required communications interface to interact with the OBC. The AMD A4-3300 can also be disregarded for similar reasons, mainly due to the scarcity of available information and its large power consumption of 65 W.

Power consumption is an important consideration when designing something meant to operate in space. Resources, such as battery capacity and the size of the solar cells, are limited on a satellite, and keeping the power consumption low is vital. To get a clearer image of the power consumption compared to the processing power of the different devices selected, the following graph was created:

![Figure 2.1: Processing power compared to power consumption for the processor candidates.](image)

For the processors marked with * in Fig. 2.1, the slowest available clock frequency have been used. As these processors have more than enough processing power for this
application, by using a slower clock frequency the power consumption will be lower.

The current power supply in the OBC has, as it stands, the capability to supply and
dissipate around 12 W to the expansion slots. The choice was made to narrow the
selection down to processors with a power consumption lower than 13 W, thus excluding
all of the processors with higher power consumption than the PC8548E.

Moving forward, the primary concern will be finding a trade-off between high perfor-
mance and reliability in space. For reliability in space, the apparent choice is the rad-hard
GR740, which also provides the SpW communication interface, simplifying the commu-
nication with the CREOLE. Radiation hardened processors, however, have a tendency
to be very expensive; the GR740 costs in the upwards of €30,000. The GR740 is also
too far below the target performance to be a good choice for this application.

For the processors not radiation hardened, the second best option is processors certified
for some level of radiation tolerance or which have been radiation tested. The PC8548E,
for instance, is on the low end of processing power and the high end with regards to
power consumption. It uses, however, Silicon On Insulator (SOI) technology and has
been graded according to the QML-Y standard by Teledyne-e2v [32].

The LS1046A, although inferior to the LS1088A in terms of power consumption, is still
the preferable choice among the two due to its military grading [29] and the fact that,
according to in-house sources, Teledyne-e2v intend to perform radiation tests on it. The
PC7448 is quickly dismissed as it, similar to the Intel Pentium III, does not possess the
required communications interfaces to communicate with the OBC.

For the remainder of the processors, the P1011, P1013, P1020 and P2020 have similar
architecture and are pin compatible with each other [33]. The P2020, with an estimated
DMIPS of 6118, has the highest processing power out of these. As the target is around
5000 DMIPS, anything lower than the P2020 is sub-optimal. Its processing power, in
combination with radiation tests at the Jet Propulsion Laboratory [34] and previous
heritage [35], makes the P2020 the superior choice among this selection of P-series pro-
cessors.

To arrive at the optimal choice of processor for this application, the remaining three
processors were compared.

• The P2020, which would provide the desired increase in performance, has been
  radiation tested at the Jet Propulsion Laboratory. It is also used in the Proton400k
  Single Board Computer (SBC) made by Space Micro and will fly on the Lunar
  IceCube mission.

• The LS1046A, which would provide more than enough processing power and has
  been military grade qualified by Teledyne-e2v.

• The PC8548E which uses SOI technology and has been QML-Y certified by Teledyne-
e2v.
Out of these three final options, the PC8548E has the highest power consumption and the lowest processing power according to Fig. 2.1. Even though it is space grade qualified, the trade-off in performance was deemed too great, and it was disregarded. The OBC will be able to supply and dissipate enough power for either of the two processors left, and the choice was made to go with the more powerful of the two remaining, the LS1046A.

2.2.5 Cooling

As the LS1046A uses flip-chip technology [10], most of the generated heat will be conducted through the lid instead of through the "legs". This might cause some problems, as heat is usually conducted through the legs of the processor, through the Printed Circuit Board (PCB), and in to the frame of the OBC. This means that heat pipes will most likely have to be used for the version that will be mounted in the OBC. Heat pipes tend to be very efficient and should have no problem with cooling the processor as long as they can be physically mounted inside the OBC.

The exact solution for this will have to be investigated if this project is taken beyond the prototype stage. For the prototype version in this project, however, a normal heat sink with a fan, as can be found in most desktop computers, will be sufficient for cooling the Central Processing Unit (CPU).

2.3 Memory

By choosing the LS1046A as the processor, the option for memory technology was limited to DDR4, see Tab. 2.2. The decision was first made to use a memory from Teledyne-e2v, as they, as stated previously, provide upscreened products and have worked with RUAG before. The only DDR4 memory Teledyne-e2v offered at the time was a 4GB Multi-Chip Module (MCM) memory, which for this application would be more than enough. By using an MCM, instead of multiple discrete chips, both space on the PCB could be saved and the signal routing and layout made easier.

However, just as the circuit design was about to start, Teledyne-e2v informed they had to make some changes to their DDR4 MCM memory, and it was not going to be available until earliest another five to six months. This meant that another memory would have to be used in this project and in the interest of saving time the decision was made to use a Dual In-line Memory Module (DIMM)-socket for DDR4 memories, along with a commercially available DDR4 memory module. The optimal choice of memory would be a specific memory module from Micron Technologies (MTA9ASF51272AZ) [36], mainly because this module comes with simulation files which will be of great use later in the design. However, the memory module of choice was no longer available for purchase, and the choice was made to instead use MTA4ATF51264AZ [37], as the two memory
modules were deemed similar enough to where the simulation results from the original memory’s files would accurately model the chip used.

2.4 Field-Programmable Gate Array

The FPGA that will be used to handle the conversion between SpW and PCIe is the SmartFusion2 (SF2) System on Chip (SoC) from Microsemi [38]. This FPGA has been used by RUAG in a previous project and is capable of performing this conversion. This solution, even though being more powerful and offering more functionality than what is needed, was chosen as RUAG’s previous experience with it would save both money and valuable time compared with designing a dedicated solution from scratch for this particular application.

2.5 Other Components

There are a number of necessary components needed by the CPU, the FPGA and the RAM, such as DC/DC converters, oscillators (for the clock) and a fanout buffer (to distribute the clock) to name a few. As these types of components are frequently used by RUAG in other projects, they already have radiation tolerant versions which can be used if this project is taken beyond the breadboard stage. For this reason, normal commercial components that could be found in the component library at RUAG were used in this project in order to save time during the component selection process.
Chapter 3

Circuit Design

The schematic was designed in DxDesigner version EE7.9.5 made by Mentor Graphics. In this chapter some parts of the schematic and certain design choices will be discussed. The full schematic can be found in Appendix B.

Figure 3.1 shows a blocks diagram of the design. The expansion card will be connected to the OBC via a connector known as a mezzanine connector, which will be the only interface between the two. The connector will provide the interface for the communication (using SpW) as well as the interface for providing power to the expansion card at 3.3 V and a bias voltage of 5 V.

The clock block will provide the reference clock needed by the system and communication clocks for the CPU, and the communication clock for the FPGA.

The FPGA will, as stated previously, act as the interface between the SpW coming from the OBC through the connector and the PCIe going to the CPU.
3.1 Central Processing Unit

The LS1046A contains several different communications interfaces, however, as the CPU will only communicate with the FPGA, most of these communication interfaces will remain unused. To communicate with the FPGA, the PCIe interface will be used. Additionally, the Inter-Integrated Circuit (I2C) interface will be used to interface with the DDR4 module’s Serial Presence Detect (SPD) pins, and the Quad Serial Peripheral Interface (QSPI) for loading boot information from an external flash drive.

The CPU allows two different voltages of the I2C interface, 3.3V and 1.8V [10]. As the voltage of the SPD pins on the DDR4 module is 2.5V [36], the pins can not simply be connected to one another without some level of voltage conversion. A bi-directional logic level converter, illustrated by Fig. 3.2, was used.² The function of this circuit is simply to convert the voltage at the I2C pins, 3.3V, to a voltage the SPD pins can manage, 2.5V.
To ensure that the CPU boots into the correct state after a reset, boot information known as the Reset Configuration Word (RCW) is read from an external device. For this application a NOR-flash memory (S25FS512S) was used and QSPI was used to interface it. A Joint Test Action Group (JTAG) connector also needs to be added to control the CPU externally, if needed, and also to program the flash-memory initially, as it will be empty at first.

The CPU contain several pins regarding the Power on Reset (POR) information, shown in Appendix B, schematic p. 5. These pins are used during a system reset to configure the CPU. It provides the CPU with information such as where the RCW can be loaded from, what type of reference clock signal will be used and the proper I/O voltage for the RAM, among other things. Most of the pins in the POR block have a weak internal pull-up resistor, so the state of the pins can be determined by pulling them to ground with a stronger pull-down resistor and mounting or dismounting the pull-down resistor to determine the pin state.

### 3.2 Clock

The CPU, as well as the PCIe interface, require a 100 MHz reference clock signal [10]. This clock signal will be provided by a low phase noise quartz-based oscillator. However, the oscillator only provides a single clock output, when four clock signals are needed. One reference clock signal is needed for the CPU system clock and two are needed for the PCIe interface (one for the CPU side and one for the FPGA side). The fourth clock signal is required by the second Serializer/Deserializer (SerDes) block in the CPU, even though it is unused [39]. Because of this a fanout buffer is used to split the signal coming from the oscillator into four separate clock signals, illustrated in Fig. 3.3.

---

2Bi-directional logic level converter design by Patrick Alberts (different transistor) ([http://cdn.sparkfun.com/datasheets/BreakoutBoards/Logic_Level_Bidirectional.pdf](http://cdn.sparkfun.com/datasheets/BreakoutBoards/Logic_Level_Bidirectional.pdf)).

"Logic_Level_Bidirectional". Released under the Creative Commons Attribute Share-Alike 3.0 License ([https://creativecommons.org/licenses/by-sa/3.0/](https://creativecommons.org/licenses/by-sa/3.0/)).
Figure 3.3: Oscillator and fanout buffer providing the 100 MHz clock references for the system.

3.3 Power

Both the CPU, DDR4 module and FPGA require multiple different voltages, according to their datasheets, [10, 40, 36], 0.6, 0.9, 1.2, 1.35, 1.8, 2.5 and 3.3 V in total. The CPU can run on a core voltage of either 0.9 or 1.0 V, as detailed in its datasheet. As the amount of power available for this card is limited, the choice was made to operate the CPU at its lowest clock frequency, at which it requires a core voltage of 0.9 V. In order to achieve these different voltages, multiple DC/DC converters were used, illustrated by Fig 3.4.
To ensure the CPU powers up correctly, the different voltages need to power up in a certain order, as detailed by its datasheet [10]. This was achieved by using the DC/DC converters power good-pins in conjunction with their enable/inhibit pins. The power good-pins send a signal when the output voltage is sufficiently high, usually $\sim 90\%$ of the target voltage, while the enable/inhibit pins halt the power up sequence until a "start signal" is received at the enable/inhibit pin. By connecting these power good-pins to the enable/inhibit pins of the subsequent DC/DC converters, the sequence at which the voltages power up can be controlled. This sequence is illustrated in Fig. 3.4. The sequence starts with the leftmost DC/DC converters (2.5 V, 1.8 V and 1.35 V) all powering up simultaneously, and is continued with the Power Good pin of the top-left DC/DC converter (2.5 V) connected do the Inhibit pin of the 3.3 V to 0.9 V DC/DC converter, which in turn has its Power Good pin connected to the top-right (1.2 V) DC/DC converter's Enable pin, and so on.

During power-up, in order to minimise the inrush current and protect the CPU, powering up the voltages slowly is preferable. This was accomplished by utilising the soft-start function on the DC/DC converters, where available.

The 0.9 V output is the core voltage of the CPU, meaning it sources most of the current and is sensitive to voltage swings. Because of this a voltage sense pin is connected between the converter and a feedback regulator pin on the CPU. This allows the converter to measure the input voltage at the CPU and compensate for any voltage drops along the way by increasing its output voltage accordingly.

During power on, the CPU and FPGA’s active-low POR pins need to be asserted (pulled low) to ensure proper start-up. This is achieved using the circuit in Fig. 3.5. As the 3.3 V source powers up, the start-up delay circuit asserts the POR pins of the CPU and FPGA until the 3.3 V source is powered up completely, and keeps it asserted for an additional amount of time, as specified by its datasheet [41], providing sufficient time for the sequence of voltages to power up, before deasserting the pin, putting the CPU and FPGA in their default operating states. A manual reset can also be performed by asserting the Manual Reset Pin, which can be done by either operating the switch or transmitting a logical zero on the External Reset Signal.
3.4 Field-Programmable Gate Array

The FPGA used for communication conversion is, as stated previously, over-dimensioned for this purpose. Most of the pins will remain unused for this application, and can be left unconnected, as a weak pull-up resistor can be designed internally according to the pinout sheet [42]. This solution was chosen in lieu of external pull-up/pull-down resistors in order to minimize the workload, as it was assumed to be less work for the ASIC department to design these internally as opposed to the layout department connecting resistors externally.

The FPGA is connected to three SpW links, accessible through the connector, and four PCIe lanes, provided by the CPU. Utilizing all of these would give the highest potential bandwidth between the expansion board and the OBC.

3.5 Layout Constraints

When designing a board, one have to take extra precaution when routing the signals to make sure no distortion takes place.

As this design contains several signals operating at high frequencies, such as the DDR4, PCIe and SpW signals, the routing of these traces will have to follow certain constraints in order to ensure proper operation. These constraints are entered into a Constraint Editor System, within DxDesigner, which will make them accessible to the layout department. Some of the constraints that need to be taken into account are: spacing, length matching and impedance matching. Impedance matching and spacing is important in order to avoid signal reflection and crosstalk, respectively. Length matching is important to ensure that the signals do not arrive at different times. For instance, when routing the 64 data signals between the CPU and DDR4 module, they have to be length-matched, both byte-wise and between bytes. If the length of two individual
bits (signals) differ too greatly, and one arrives at the receiver well before the other as a result, correctly timing the reading of the byte will be difficult and error-prone.

In order to mitigate voltage spikes on the signals due to interference, some signals are differential. These signals are routed in parallel and close to one another, so that any external disturbance causing a voltage spike on one of the signals is felt equally at the other. When reading these signals at the receiver, the difference is calculated and any such spike thereby removed.

For certain high current sourcing connections, specifically the VDD trace, a short, low impedance path is desirable as the voltage drop increases with increasing current.
Chapter 4

Simulations

Prior to ordering and manufacturing the PCB, simulations are performed to evaluate the signal integrity of the board. The simulations are made using HyperLynx VX.2.5 by Mentor Graphics. This simulation software makes it possible to test different values of the components used and different On-Die Termination (ODT) (toggleable termination resistors inside the chip), using a simulated oscilloscope to measure frequencies, voltages, eye diagrams and more.

In order to simulate driver and receiver characteristics, a type of file called IBIS (Input/Output Buffer Information Specification) file is commonly used. These files are provided by the Integrated Circuit (IC) manufacturers and are a way to provide driver and receiver characteristics without disclosing too much information regarding the specifics of the IC.

No simulations were made for the SpW and PCIe signals; at RUAG, it has been decided that as long as the layout constraints for routing SpW and PCIe are followed, no simulations of the signal integrity are needed.

4.1 System Clock

The system uses a 100 MHz reference clock for both the core clock to the CPU and the reference clock to the PCIe. The voltage levels of these signals are determined by a number of serial and parallel termination resistors. (The specific serial resistors, controlling the AC level, and parallel resistors, controlling the DC level, are R09012-R09019 and R03023-R03024 respectively and can be seen in Appendix B schematic p.9 and p.3.) These clock signals were simulated in order to determine whether they fall within the specifications of the receivers.
The specifications for the LS1046A core differential clock input are a differential voltage swing between 100-600 mV and a common mode voltage between 50-1570 mV [10]. As can be seen in Fig. 4.1, the common mode voltage is within the specified range but the differential voltage swing is too large.

To lower the voltage swing to within the allowed range, the serial resistors for this clock signal (R09018 and R09019 in Appendix B schematic p.9) were increased. This resulted in the clock signal meeting the voltage swing requirement, as can be seen in Fig. 4.2.

Figure 4.1: LS1046A core clock input, single ended signals and differential, with original component values.
The differential clock inputs for the SerDes blocks, being AC-coupled, does not have any requirement for a common mode voltage level. There is, however, a requirement that the differential voltage swing is within 200-800 mV [10].
Figure 4.3: LS1046A SerDes clock input, single ended signals and differential, with original component values.

As can be seen in Fig. 4.3, the differential voltage swing is larger than the allowed range of the device. To mitigate this, the values of this clock signal’s serial resistors (R09012-R09015 in Appendix B schematic p.9) were increased. The resulting waveforms can be seen in Fig. 4.4.
4.2 Memory Interface

As stated earlier in section 2.3, the simulation files used are from a different memory module than the one used on the board, however, it was deemed similar enough to provide valuable simulation results. Notable differences between the module used on the board and the one used in the simulations include the absence of Error Correcting Code (ECC) and four memory chips instead of nine.

As this application uses a commercially available memory module, all of the necessary termination circuitry already exists on the module. This means that the memory module is connected directly to the CPU with no components in the signal path. Therefore, the simulations of this part serve to verify that the layout has been done correctly and that all of the signal constraints have been followed. In cases where the signals do not fulfill the timing and voltage constraints, different values of the ODT can be used to tune the signals accordingly.

Ideally, most of the signals should be simulated before sending the schematic to the PCB manufacturer, so any mistakes in signal routing and such can be remedied beforehand.
Due to time constraints, only a few signals could be simulated and the most critical signals were chosen. These signals were the strobe, data, clock and chip select.

### 4.2.1 Clock

The reference clock for the memory is generated and provided by the CPU to the memory module. It is then distributed to all nine of the memory chips in series. This signal has to follow a number of requirements found in the datasheet for the memory chip used on the module [43].

- The single ended signals must be between GND and 1.2 V.
- The differential signal must go above 400 mV on the positive half cycle and below -400 mV on the negative half cycle.
- The differential signal must have a monotonic slope on the rising edge in the region -150 mV to 400 mV, and on the falling edge between 150 mV and -400 mV. The ±150 mV-levels are marked with dotted lines in Fig. 4.5a.

![Differential signal](image1)

**Figure 4.5:** Clock signal for the first three memory chips on the module.

In Fig. 4.5 one can see that the clock signal satisfies the stated requirements. For clarity, only three are shown, although all nine were simulated and confirmed to satisfy the requirements.

### 4.2.2 Data and Strobe

In DDR4 memories, a data strobe signal is used when transferring data to and from the RAM. The data strobe signal is essentially a clock signal that acts as a data valid flag,
informing the CPU’s memory controller when data is available to read or write. One strobe signal is used per byte of addressable memory. The crucial constraints for the data strobe(s) are:

- The differential signal (red in Fig. 4.6) needs to reach a minimum of ±186 mV.
- The crossing point of the single ended signals needs to be between 0.679 - 1.125 V.
- The single-ended signals (green and blue in Fig. 4.6) can not exceed 1.2 V nor go below GND, with exception to over-/undershoot specifications, as detailed in the data sheet [43].

The datasheet specifies the maximum allowed overshoot to 240 mV (above 1.2 V), and as can be seen in the figure below the signal is well within this limit.

![Data strobe signal, single ended signals and differential signal.](image)

**Figure 4.6:** Data strobe signal, single ended signals and differential signal.

As can be seen in Fig. 4.6, the strobe signals, in both directions, are "clean" with close to no distortion, ripple or voltage spikes. One can also see that the signals stays within the specifications stated above.

When plotting data signals, it is common to use an eye diagram to evaluate the signal integrity. In order to successfully read and decode the signal, it needs to follow the specifications found in the datasheet [43]. The crucial specifications/constraints can be visualised as a "mask" when simulating the signal, shown in blue in the figures below. The signal should not cross the marked area of the mask.
Both the memory and the CPU has a number of different selections for ODT. The simulations that can be seen in Fig. 4.7 were performed with ODT disabled for both the memory and the CPU and one can clearly see that the signals are crossing the mask.

To improve the signals, different values of ODT were tested until the simulation yielded a result where the signals stayed clear of the mask. As can be seen in Fig. 4.8, the signals are within the specifications when using 34 and 60 Ohm termination for the memory and the CPU respectively.

**Figure 4.7:** Eye diagram of the data signal with no ODT.

**Figure 4.8:** Eye diagram of the data signal tuned with ODT.
4.2.3 Chip Select

The chip select is a command signal used for "activating" the memory when reading and writing data. As chip select is an active low signal, the memory will be active when the signal is low and inactive when the signal is high.

![Chip select signals for the memory chips on the DDR4 module.](image)

(a) Rising edge response.  (b) Falling edge response.

**Figure 4.9:** Chip select signals for the memory chips on the DDR4 module.

As can be seen in Fig. 4.9, there is quite a bit of ringing (that is, the signal oscillates for a while after the step) on the inputs to the memory modules. When the signal goes from high to low, Fig. 4.9b, this is not a problem as the level at which the signal is interpreted as low is 500 mV. However, when the signal goes from low to high, Fig. 4.9a, the level at which the signal is interpreted as high is 700 mV. Some of the signals cross below this level due to the ringing, however they do not cross the allowed ring back level at 675 mV [43] so no action was taken to improve the signal.
Chapter 5

Tests

Once the PCB had been manufactured and all the components mounted, some simple hardware tests should be performed before handing it off to the software department. These tests consist of checking that the voltages are in their specified ranges, the power-up sequence performs as intended, and the clock signals look good.

5.1 Voltages

The first time the board was powered up, the input voltage (3.3 V) was brought up slowly. This was done in order to detect if there was, for example, a short somewhere on the board, whilst the supply was still at a relatively low voltage.

Once the board had been powered up completely, the voltages from the DC/DC converters were measured. As can be seen in Tab. 5.1, all of the voltages are well within their required levels.

**Table 5.1: Voltages from the DC/DC converters**

<table>
<thead>
<tr>
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<td>2.5 (± 0.125)</td>
<td>2.490</td>
<td>[10]</td>
</tr>
<tr>
<td>1.8 (± 0.09)</td>
<td>1.801</td>
<td>[10]</td>
</tr>
<tr>
<td>1.35 (± 0.067)</td>
<td>1.351</td>
<td>[10]</td>
</tr>
<tr>
<td>0.9 (± 0.03)</td>
<td>0.903</td>
<td>[10]</td>
</tr>
<tr>
<td>1.2 (± 0.06)</td>
<td>1.197</td>
<td>[10]</td>
</tr>
<tr>
<td>0.6 (± 0.032)</td>
<td>0.599</td>
<td>[37]</td>
</tr>
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</table>
5.2 Power-Up Sequence

To ensure that the voltages are powered up sequentially, as detailed in Section 3.3, the output of the converters were measured as power was applied to the board. The power up sequence is as follows: 2.5 V, 1.8 V, 1.35 V → 0.9 V → 1.2 V → 0.6 V, with each section needing to reach 90% of its output voltage before the subsequent section reaches 10%. The following figures show the voltages measured during the power-up sequence.

![Figure 5.1: Power-up of the 2.5 V (yellow) and the 0.9 V (cyan) outputs.](image-url)
As can be seen by Fig. 5.1-5.3, all of the voltages are powered up in the correct order. It can also be seen that the converters complete their own power-up before the next converter in the sequence starts powering up.
Figure 5.4: POR signal (cyan) deasserted after the last converter (0.6 V, yellow) has powered up.

Figure 5.4 shows that the POR signal is being held asserted (low) until well after the last converter has powered up, giving all converters enough time to start up before the POR signal is deasserted, allowing the CPU and FPGA to enter normal operation.

5.3 Clock Signals

Measuring the CPU system clock signals directly at the CPU’s pins is extremely difficult as the CPU is of the type “Ball Grid Array” (the pins are located between the CPU and PCB). Measuring the signal close to the pin is also difficult without distorting it, as the final signal is of a relatively low voltage, and at a high frequency (∼ 200 mV, 100 MHz, see Fig. 4.2). The signal was able to be measured at the output of the fanout buffer without major distortions, as can be seen in Fig. 5.5.
Figure 5.5: CPU core clock signal at the output of the fanout buffer, single ended signals (cyan and yellow) and differential (red).
Chapter 6

Conclusions and Future Work

From the tests that could be performed, outlined in the previous chapter, all of the voltages are well within their allowed range. The start-up sequence is also working properly, with no subsequent converters power-up overlapping with a previous one. The measured clock signal, however, is difficult to judge as either good or bad when it comes to the voltage levels as there are no requirements on the signal at this point in the circuit. Because of this, a simulation of the clock signal was performed at the same point in the circuit in order to verify both that the simulations performed in chapter 4 will be close to what is actually measured and that the measured clock will be at a good level when it enters the CPU.
By comparing the simulated signal in Fig. 6.1 with the measured signal in Fig. 5.5 one can see that the measured signal, apart from a bit of distortion, matches quite well with the simulation. The distortion in the measured signal is most likely due to a rather poor test setup. With a better test setup and by using proper differential probes (which are made to measure this type of signal), it is possible that the measured signal would be less distorted.

The comparison between the measured and simulated clock signal (Fig. 5.5 and 6.1) does give some confidence that the rest of the simulations will be relatively accurate.

One flaw in the design of the board is the lack of debugging utilities. When the time came to program the FPGA and CPU, a lack of various common debugging interfaces was noted by the software team, such as a Universal Asynchronous Receiver Transmitter (UART) interface, or even simple LEDs to indicate the status of the board. Adding these would have been trivial during the design of the board, and would have been of great help to the software team. This was unfortunately something that was overlooked by everyone involved in the design of the board.

When the expansion board had been handed off to the software department to be programmed, they were not able to take control of the CPU. It was found that the reason for this is most likely a faulty connection between two signals of the programming (JTAG)
interface. This is something that can be modified on the PCB and would hopefully solve the problem. There was, however, not enough time left to get that modification done before the conclusion of this thesis.

Even though a performance test was not able to be carried out, there should not be a problem to achieve the desired 5000 DMIPS with this processor. The only notable limitation on the performance in this application is the communication between the processor and the OBC, which, depending on how the communication is utilized, should not lower the performance from the theoretical 22560 DMIPS to 5000 DMIPS or below.

When further developing this project beyond the breadboard stage, using a DIMM socket for the memory will not suffice. In a flight-ready model, the memory will have to consist of discrete chips soldered onto the PCB, much like how the DIMM looks like externally. Termination resistors and decoupling capacitors currently located on the DIMM would also need to be added directly to the PCB. In this case, the simulations conducted in this thesis would be invalid and would need to be repeated with the new configuration.

6.1 Future Work

6.1.1 Testing

The next step in the development of the expansion card is to properly test all of the functionality, making sure that the processor can communicate with the OBC and that the memory module works as intended. A performance test is also needed in order to find out the actual processing power of the board.

It is also important to determine the total power consumption, as well as to monitor the voltages and make sure they are stable when significant current is drawn.

6.1.2 Software

In order for the board to be properly tested and, eventually, work as intended, software needs to be developed. The developing of this software was beyond the scope of this thesis, and it was intended that the software department at RUAG would provide it. Due to time constraints, this software could not be delivered in time and the board had to be evaluated without it. This means the communication, data handling and performance could not be evaluated properly by this thesis.
6.1.3 Heat Pipes

Another area that needs to be investigated further is the solution for using heat pipes as a cooling solution. This would require the system, the coprocessor board mounted in the OBC, to be modelled so that a thermal analysis can be performed. This would allow one to determine the size, the number and the type of heat pipes needed for this application.
Bibliography


[40] Microsemi, ”IGLOO2 FPGA and SmartFusion2 SoC FPGA”, SmartFusion2 Datasheet, Rev. 12, 08/2018.


Micron, "Automotive DDR4 SDRAM, MT40A512M8, MT40A256M16”, DDR4 Memory Chip Datasheet, Rev. I, 05/19.

Appendices
## Appendix A

### Complete table of processors

**Table A.1:** Complete table of the processors evaluated

<table>
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1Based on PowerPC processors with the same core (P2020, e500 core).
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</table>
Appendix B

Schematic

The pages of the schematic (which is the rest of the pages in the thesis) has the format A3 paper in landscape orientation.
Third party contravention will be prosecuted.